

OptiMOS® Power-Transistor

Feature

- N-Channel
- Enhancement mode
- Excellent Gate Charge x $R_{DS(on)}$ product (FOM)
- Superior thermal resistance
- 175°C operating temperature
- Avalanche rated
- dv/dt rated

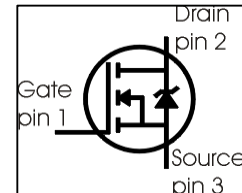
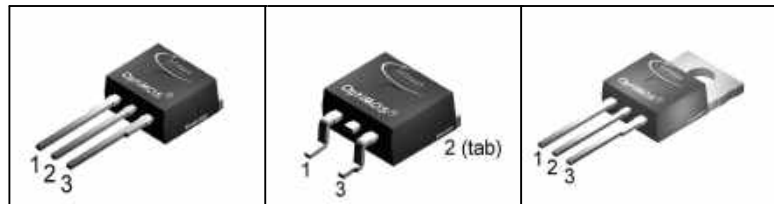
Product Summary

V_{DS}	30	V
$R_{DS(on)}$ max. SMD version	3.1	mΩ
I_D	80	A

P- TO262 -3-1

P- TO263 -3-2

P- TO220 -3-1



Type	Package	Ordering Code	Marking
SPP80N03S2-03	P- TO220 -3-1	Q67040-S4247	2N0303
SPB80N03S2-03	P- TO263 -3-2	Q67040-S4258	2N0303
SPI80N03S2-03	P- TO262 -3-1	Q67042-S4079	2N0303

Maximum Ratings, at $T_j = 25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Value	Unit
Continuous drain current 1) $T_C=25^\circ\text{C}$	I_D	80 80	A
Pulsed drain current $T_C=25^\circ\text{C}$	$I_{D \text{ puls}}$	320	
Avalanche energy, single pulse $I_D=80 \text{ A}$, $V_{DD}=25\text{V}$, $R_{GS}=25\Omega$	E_{AS}	810	mJ
Repetitive avalanche energy, limited by $T_{jmax}^{2)}$	E_{AR}	30	
Reverse diode dv/dt $I_S=80\text{A}$, $V_{DS}=24\text{V}$, $di/dt=200\text{A}/\mu\text{s}$, $T_{jmax}=175^\circ\text{C}$	dv/dt	6	kV/ μs
Gate source voltage	V_{GS}	± 20	V
Power dissipation $T_C=25^\circ\text{C}$	P_{tot}	300	W
Operating and storage temperature	T_j, T_{stg}	-55... +175	°C
IEC climatic category; DIN IEC 68-1		55/175/56	

Thermal Characteristics

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Characteristics					
Thermal resistance, junction - case	R_{thJC}	-	0.3	0.5	K/W
Thermal resistance, junction - ambient, leaded	R_{thJA}	-	-	62	
SMD version, device on PCB: @ min. footprint @ 6 cm ² cooling area ³⁾	R_{thJA}	-	-	62 40	

Electrical Characteristics, at $T_j = 25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Static Characteristics					
Drain-source breakdown voltage $V_{GS}=0V, I_D=1mA$	$V_{(BR)DSS}$	30	-	-	V
Gate threshold voltage, $V_{GS} = V_{DS}$ $I_D=250\mu A$	$V_{GS(th)}$	2.1	3	4	
Zero gate voltage drain current $V_{DS}=30V, V_{GS}=0V, T_j=25^\circ\text{C}$ $V_{DS}=30V, V_{GS}=0V, T_j=125^\circ\text{C}$	I_{DSS}	-	0.01	1	μA
		-	1	100	
Gate-source leakage current $V_{GS}=20V, V_{DS}=0V$	I_{GSS}	-	1	100	nA
Drain-source on-state resistance ⁴⁾ $V_{GS}=10V, I_D=80A$ $V_{GS}=10V, I_D=80A, \text{SMD version}$	$R_{DS(on)}$	-	2.6	3.4	m Ω
		-	2.3	3.1	

¹Current limited by bondwire ; with an $R_{thJC} = 0.5K/W$ the chip is able to carry $I_D = 307A$ at 25°C , for detailed information see app.-note ANPS071E available at www.infineon.com/optimos

²Defined by design. Not subject to production test.

³Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical without blown air.

⁴Diagrams are related to straight lead versions

Electrical Characteristics

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic Characteristics

Transconductance	g_{fs}	$V_{DS} \geq 2 \cdot I_D \cdot R_{DS(on)max}$, $I_D = 80A$	66	132	-	S
Input capacitance	C_{iss}	$V_{GS} = 0V$, $V_{DS} = 25V$, $f = 1MHz$	-	5280	7020	pF
Output capacitance	C_{oss}		-	2420	3220	
Reverse transfer capacitance	C_{rss}		-	470	700	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 15V$, $V_{GS} = 10V$, $I_D = 80A$, $R_G = 2.2\Omega$	-	22	33	ns
Rise time	t_r		-	325	490	
Turn-off delay time	$t_{d(off)}$		-	90	140	
Fall time	t_f		-	110	160	

Gate Charge Characteristics

Gate to source charge	Q_{gs}	$V_{DD} = 24V$, $I_D = 80A$	-	26	34	nC
Gate to drain charge	Q_{gd}		-	45	68	
Gate charge total	Q_g	$V_{DD} = 24V$, $I_D = 80A$, $V_{GS} = 0$ to $10V$	-	110	150	
Gate plateau voltage	$V_{(plateau)}$	$V_{DD} = 24V$, $I_D = 80A$	-	5.2	-	V

Reverse Diode

Inverse diode continuous forward current	I_S	$T_C = 25^\circ C$	-	-	80	A
Inv. diode direct current, pulsed	I_{SM}		-	-	320	
Inverse diode forward voltage	V_{SD}	$V_{GS} = 0V$, $I_F = 80A$	-	0.9	1.3	V
Reverse recovery time	t_{rr}	$V_R = 15V$, $I_F = 8A$, $di_F/dt = 100A/\mu s$	-	65	80	ns
Reverse recovery charge	Q_{rr}		-	87	110	