N-channel vertical D-MOS transistor 2N7002

FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT23 envelope. It is designed for use as a Surface Mounted Device (SMD) in thin and thick-film circuits, with applications in relay, high-speed and line transformer drivers.

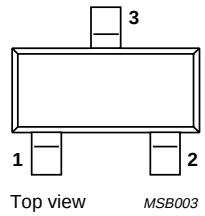
PINNING - SOT23

PIN	DESCRIPTION
1	gate
2	source
3	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
V_{DS}	drain-source voltage		60	V
I_D	drain current	DC value	180	mA
$R_{DS(on)}$	drain-source on-resistance	I_D = 500 mA V_{GS} = 10 V	5	Ω
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{GS} = V_{DS}	3	V

PIN CONFIGURATION



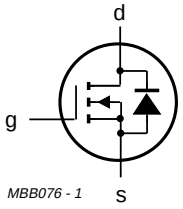


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Fig.1 Simplified outline and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	60	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	40	V
I_D	drain current	DC value	–	180	mA
I_{DM}	drain current	peak value	–	800	mA
P_{tot}	total power dissipation	T_{amb} = 25 °C (note 1) (note 2)	 – –	 300 250	 mW mW
T_{stg}	storage temperature range		–65	150	°C
T_j	junction temperature		–	150	°C

Notes

1. Mounted on a ceramic substrate measuring $10 \times 8 \times 0.7$ mm.
2. Mounted on a printed circuit board.

THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient	note 1 note 2	430 500	K/W K/W

Notes

1. Mounted on a ceramic substrate measuring $10 \times 8 \times 0.7$ mm.
2. Mounted on a printed circuit board.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 μA V_{GS} = 0	60	90	–	V
I_{DSS}	drain-source leakage current	V_{DS} = 48 V V_{GS} = 0	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	V_{DS} = 0 $\pm V_{GS}$ = 15 V	–	–	10	nA
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA V_{GS} = V_{DS}	0.8	–	3	V
$R_{DS(on)}$	drain-source on-resistance	I_D = 500 mA V_{GS} = 10 V	–	3.5	5	Ω
		I_D = 75 mA V_{GS} = 4.5 V	–	–	5.3	Ω
$\lvert Y_{fs} \rvert$	transfer admittance	I_D = 200 mA V_{DS} = 10 V	100	200	–	mS
C_{iss}	input capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	25	40	pF
C_{oss}	output capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	22	30	pF
C_{rss}	feedback capacitance	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz	–	6	10	pF
Switching times (see Figs 2 **and** 3**)**						
t_{on}	turn-on time	I_D = 200 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	–	10	ns
t_{off}	turn-off time	I_D = 200 mA V_{DD} = 50 V V_{GS} = 0 to 10 V	–	–	15	ns