RENESAS

MOS FIELD EFFECT POWER TRANSISTOR

Phase-out/Discontinued

2SK1758

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

DESCRIPTION

The 2SK1758 is N-channel MOS Field Effect Transistor designed for high voltage switching applications.

FEATURES

- Low On-state Resistance
  $R_{DS(on)}$ = 4.2 Ω (V_{GS} = 10 V, I_D = 1 A)
- Low C_{iss} C_{iss} = 360 pF TYP.
- Built-in G-S Gate Protection Diode
- High Avalanche Capability Ratings

QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

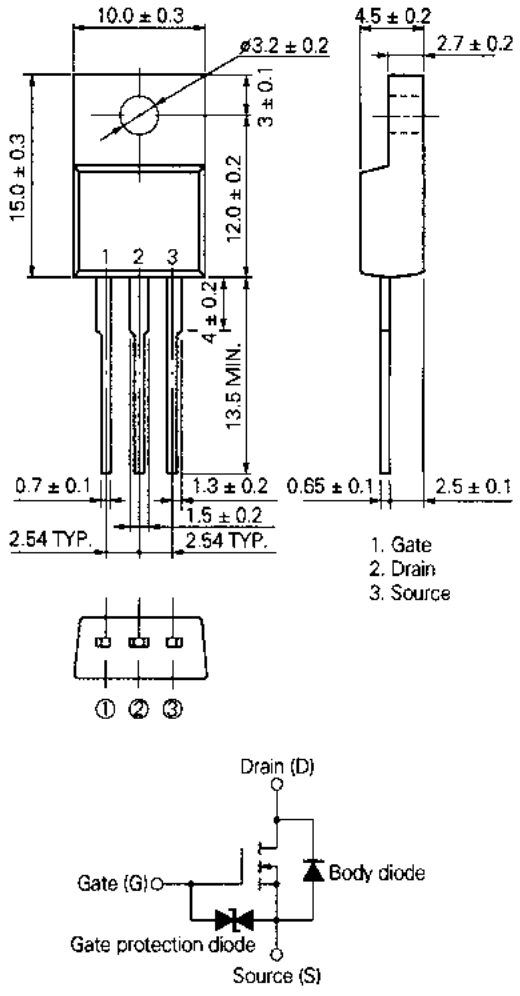
ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Drain to Source Voltage	V_{DSS}	600	V
Gate to Source Voltage	V_{GSS}	±30	V
Drain Current (DC)	$I_{D(DC)}$	±2.0	A
Drain Current (pulse)	$I_{D(pulse)}$*	±8.0	A
Total Power Dissipation (T_C = 25 °C)	P_{T1}	30	W
Total Power Dissipation (T_a = 25 °C)	P_{T2}	2.0	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−55 to +150	°C
Single Avalanche Current	I_{AS}**	3.0	A
Single Avalanche Energy	E_{AS}**	96	mJ

* PW ≦ 10 μs, Duty Cycle ≦ 1 %

** Starting T_{ch} = 25 °C, R_G = 25 Ω, V_{GS} = 20 V → 0

PACKAGE DIMENSIONS
(in millimeters)

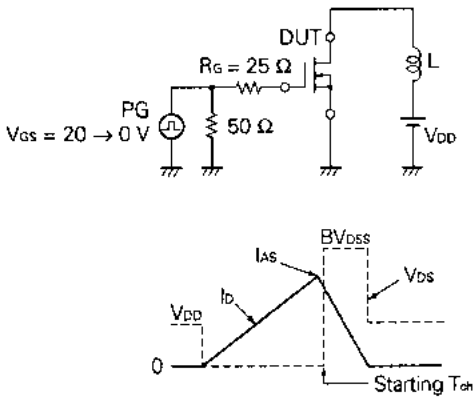


Document No. TC-2436
Date Published August 1993 M
Printed in Japan

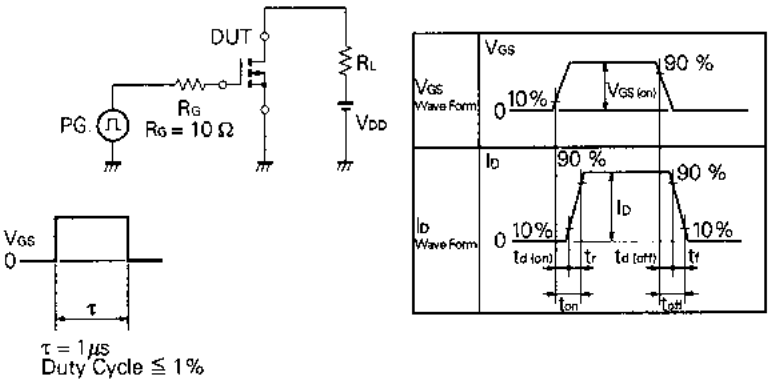
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	$R_{DS(on)}$		2.8	4.2	Ω	V_{GS} = 10 V, I_D = 1 A
Gate to Source Cutoff Voltage	$V_{GS(off)}$	2.0		4.0	V	V_{DS} = 10 V, I_D = 1 mA
Forward Transfer Admittance	$\|y_{fs}\|$	0.5	1.3		S	V_{DS} = 10 V, I_D = 1 A
Drain Leakage Current	I_{DSS}			100	μA	V_{DS} = 600 V, V_{GS} = 0
Gate to Source Leakage Current	I_{GSS}			±10	μA	V_{GS} = ±30 V, V_{DS} = 0
Input Capacitance	C_{iss}		360		pF	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz
Output Capacitance	C_{oss}		130		pF	
Reverse Transfer Capacitance	C_{rss}		50		pF	
Turn-On Delay Time	$t_{d(on)}$		5		ns	$V_{GS(on)}$ = 10 V V_{DD} = 150 V I_D = 1 A, R_G = 10 Ω R_L = 150 Ω
Rise Time	t_r		6		ns	
Turn-Off Delay Time	$t_{d(off)}$		60		ns	
Fall Time	t_f		20		ns	
Total Gate Charge	Q_G		17		nC	V_{GS} = 10 V I_F = 2 A V_{DD} = 400 V
Gate to Source Charge	Q_{GS}		3		nC	
Gate to Drain Charge	Q_{GD}		10		nC	
Diode Forward Voltage	$V_{F(S-D)}$		0.85		V	I_F = 2 A, V_{GS} = 0
Reverse Recovery Time	t_{rr}		270		ns	I_F = 2 A, V_{GS} = 0 di/dt = 50 A/μs
Reverse Recovery Charge	Q_{rr}		1.4		μC	

Test Circuit 1: Avalanche Capability



Test Circuit 2: Switching Time



Test Circuit 3: Gate Charge