NEC

MOS FIELD EFFECT TRANSISTOR

2SK2141

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

DESCRIPTION

The 2SK2141 is N-channel Power MOS Field Effect Transistor designed for high voltage switching applications.

FEATURES

- Low On-state Resistance
  $R_{DS(on)}$ = 1.1 Ω MAX. (V_{GS} = 10 V, I_D = 3.0 A)
- Low C_{iss} C_{iss} = 1150 pF TYP.
- High Avalanche Capability Ratings
- Isolated TO-220 (MP-45F) Package

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Drain to Source Voltage	V_{DSS}	600	V
Gate to Source Voltage	V_{GSS}	±30	V
Drain Current (DC)	$I_{D(DC)}$	±6.0	A
Drain Current (pulse)	$I_{D(pulse)}$*	±24	A
Total Power Dissipation (T_C = 25 °C)	P_{T1}	35	W
Total Power Dissipation (T_a = 25 °C)	P_{T2}	2.0	W
Storage Temperature	T_{stg}	–55 to +150	°C
Channel Temperature	T_{ch}	150	°C
Single Avalanche Current	I_{AS}**	6.0	A
Single Avalanche Energy	E_{AS}**	12	mJ

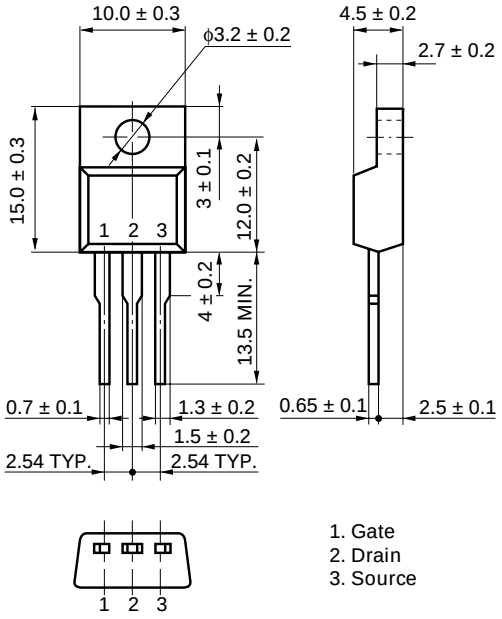
*PW ≤ 10 μs, Duty Cycle ≤ 1%

**Starting T_{ch} = 25 °C, R_G = 25 Ω, V_{GS} = 20 V → 0

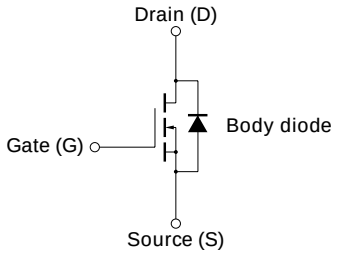
The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device is actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

PACKAGE DIMENSIONS

(in millimeters)



ISOLATED TO-220 (MP-45F)



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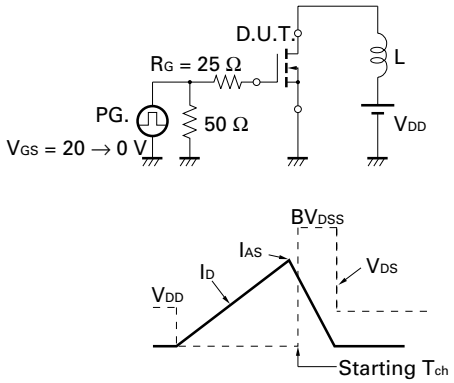
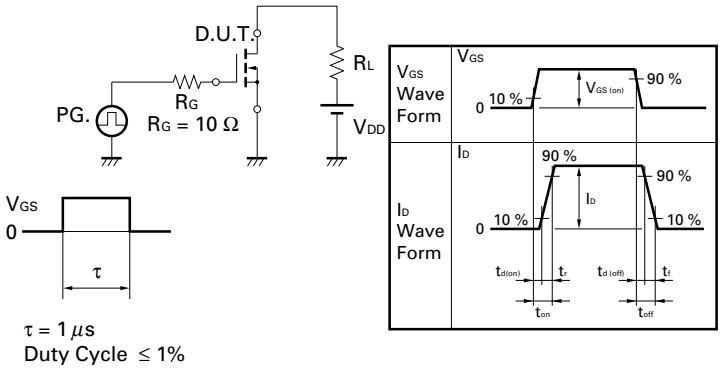
ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	$R_{DS(on)}$		0.8	1.1	Ω	V_{GS} = 10 V, I_D = 3.0 A
Gate to Source Cutoff Voltage	$V_{GS(off)}$	2.5		3.5	V	V_{DS} = 10 V, I_D = 1 mA
Forward Transfer Admittance	$\|y_{fs}\|$	2.0			S	V_{DS} = 10 V, I_D = 3.0 A
Drain Leakage Current	I_{DSS}			100	μA	V_{DS} = 600V, V_{GS} = 0
Gate to Source Leakage Current	I_{GSS}			±100	nA	V_{GS} = ±30 V, V_{DS} = 0
Input Capacitance	C_{iss}		1150		pF	V_{DS} = 10 V
Output Capacitance	C_{oss}		260		pF	V_{GS} = 0
Reverse Transfer Capacitance	C_{rss}		60		pF	f = 1 MHz
Turn-On Delay Time	$t_{d(on)}$		15		ns	V_{GS} = 10 V
Rise Time	t_r		15		ns	V_{DD} = 150 V
Turn-Off Delay Time	$t_{d(off)}$		75		ns	I_D = 3.0 A, R_G = 10 Ω
Fall Time	t_f		13		ns	R_L = 37.5 Ω
Total Gate Charge	Q_G		40		nC	V_{GS} = 10 V
Gate to Source Charge	Q_{GS}		6.0		nC	I_D = 6.0 A
Gate to Drain Charge	Q_{GD}		20		nC	V_{DD} = 480 V
Diode Forward Voltage	$V_{F(S-D)}$		1.0		V	I_F = 6.0 A, V_{GS} = 0
Reverse Recovery Time	t_{rr}		370		ns	I_F = 6.0 A
Reverse Recovery Charge	Q_{rr}		1.5		μC	di/dt = 50 A/μs

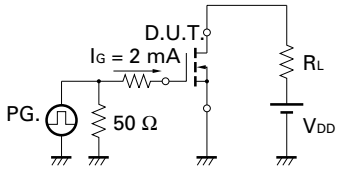
Test Circuit 1: Avalanche Capability



Test Circuit 2: Switching Time



Test Circuit 3: Gate Charge



The application circuits and their parameters are for references only and are not intended for use in actual design-in's.