FAIRCHILD SEMICONDUCTOR®

May 2001

QFET™

FQB85N06 / FQI85N06

60V N-Channel MOSFET

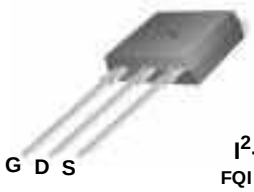
General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for low voltage applications such as automotive, DC/DC converters, and high efficiency switching for power management in portable and battery operated products.

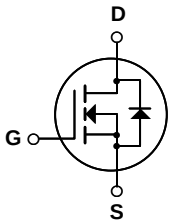
Features

- 85A, 60V, $R_{DS(on)}$ = 0.010Ω @V_{GS} = 10 V
- Low gate charge (typically 86 nC)
- Low Crss (typically 165 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
- 175°C maximum junction temperature rating

D^2-PAK
FQB Series



I^2-PAK
FQI Series



Absolute Maximum Ratings

T_C = 25°C unless otherwise noted

Symbol	Parameter		FQB85N06 / FQI85N06	Units
V_{DSS}	Drain-Source Voltage		60	V
I_D	Drain Current - Continuous (T_C = 25°C)		85	A
	- Continuous (T_C = 100°C)		60	A
I_{DM}	Drain Current - Pulsed	(Note 1)	300	A
V_{GSS}	Gate-Source Voltage		± 25	V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	810	mJ
I_{AR}	Avalanche Current	(Note 1)	85	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	16.0	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	7.0	V/ns
P_D	Power Dissipation (T_A = 25°C) *		3.75	W
	Power Dissipation (T_C = 25°C)		160	W
	- Derate above 25°C		1.07	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +175	°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300	°C

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	0.94	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient *	--	40	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	62.5	°C/W

* When mounted on the minimum pad size recommended (PCB Mount)

©2001 Fairchild Semiconductor Corporation

Electrical Characteristics

T_C = 25°C unless otherwise noted

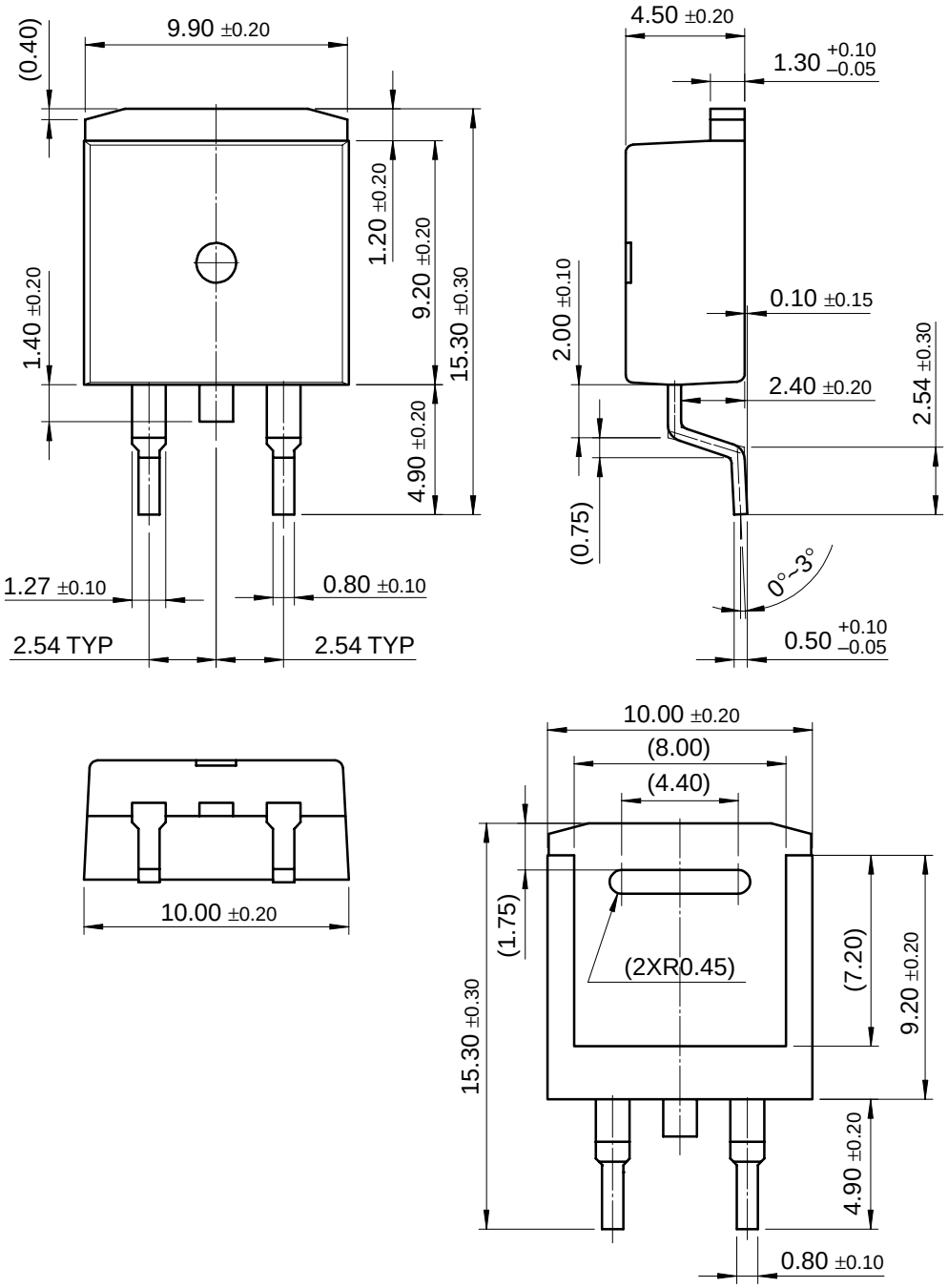
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	60	--	--	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	--	0.06	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 60 V, V_{GS} = 0 V	--	--	1	μA
		V_{DS} = 48 V, T_C = 150°C	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 25 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -25 V, V_{DS} = 0 V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 42.5 A	--	0.008	0.010	Ω
g_{FS}	Forward Transconductance	V_{DS} = 25 V, I_D = 42.5 A (Note 4)	--	54	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	3170	4120	pF
C_{oss}	Output Capacitance		--	1150	1500	pF
C_{rss}	Reverse Transfer Capacitance		--	165	220	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 30 V, I_D = 42.5 A, R_G = 25 Ω (Note 4, 5)	--	40	90	ns
t_r	Turn-On Rise Time		--	230	470	ns
$t_{d(off)}$	Turn-Off Delay Time		--	175	360	ns
t_f	Turn-Off Fall Time		--	170	350	ns
Q_g	Total Gate Charge	V_{DS} = 48 V, I_D = 85 A, V_{GS} = 10 V (Note 4, 5)	--	86	112	nC
Q_{gs}	Gate-Source Charge		--	20.5	--	nC
Q_{gd}	Gate-Drain Charge		--	36	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	85	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	300	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 85 A	--	--	1.5	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 85 A, dI_F / dt = 100 Aμ/s (Note 4)	--	70	--	ns
Q_{rr}	Reverse Recovery Charge		--	135	--	nC

Notes:
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 130μH, I_{AS} = 85A, V_{DD} = 25V, R_G = 25 Ω, Starting T_J = 25°C
3. $I_{SD} \leq$ 85A, di/dt $\leq$ 300A/μs, $V_{DD} \leq BV_{DSS}$, Starting T_J = 25°C
4. Pulse Test : Pulse width $\leq$ 300μs, Duty cycle $\leq$ 2%
5. Essentially independent of operating temperature
6. Continuous Drain Current Calculated by Maximum Junction Temperature : Limited by Package

©2001 Fairchild Semiconductor Corporation

Package Dimensions

D^2PAK



©2001 Fairchild Semiconductor Corporation