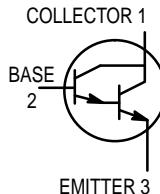


Darlington Transistors

NPN Silicon

BC517



CASE 29-04, STYLE 17
TO-92 (TO-226AA)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CES}	30	Vdc
Collector-Base Voltage	V_{CB}	40	Vdc
Emitter-Base Voltage	V_{EB}	10	Vdc
Collector Current — Continuous	I_C	1.0	Adc
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	625 12	mW mW/ $^\circ\text{C}$
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	1.5 12	Watts mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	$^\circ\text{C/W}$
Thermal Resistance, Junction to Case	$R_{\theta JC}$	83.3	$^\circ\text{C/W}$

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Collector-Emitter Breakdown Voltage ($I_C = 2.0 \text{ mA dc}, V_{BE} = 0$)	$V_{(BR)CES}$	30	—	—	Vdc
Collector-Base Breakdown Voltage ($I_C = 10 \mu\text{A dc}, I_E = 0$)	$V_{(BR)CBO}$	40	—	—	Vdc
Emitter-Base Breakdown Voltage ($I_E = 100 \text{ nA dc}, I_C = 0$)	$V_{(BR)EBO}$	10	—	—	Vdc
Collector Cutoff Current ($V_{CE} = 30 \text{ Vdc}$)	I_{CES}	—	—	500	nAdc
Collector Cutoff Current ($V_{CB} = 30 \text{ Vdc}, I_E = 0$)	I_{CBO}	—	—	100	nAdc
Emitter Cutoff Current ($V_{EB} = 10 \text{ Vdc}, I_C = 0$)	I_{EBO}	—	—	100	nAdc

Characteristic	Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS(1)					
DC Current Gain ($I_C = 20 \text{ mA}_\text{dc}$, $V_{CE} = 2.0 \text{ V}_\text{dc}$)	h_{FE}	30,000	—	—	—
Collector-Emitter Saturation Voltage ($I_C = 100 \text{ mA}_\text{dc}$, $I_B = 0.1 \text{ mA}_\text{dc}$)	$V_{CE(\text{sat})}$	—	—	1.0	V_dc
Base-Emitter On Voltage ($I_C = 10 \text{ mA}_\text{dc}$, $V_{CE} = 5.0 \text{ V}_\text{dc}$)	$V_{BE(\text{on})}$	—	—	1.4	V_dc
SMALL-SIGNAL CHARACTERISTICS					
Current-Gain — Bandwidth Product ⁽²⁾ ($I_C = 10 \text{ mA}_\text{dc}$, $V_{CE} = 5.0 \text{ V}_\text{dc}$, $f = 100 \text{ MHz}$)	f_T	—	200	—	MHz

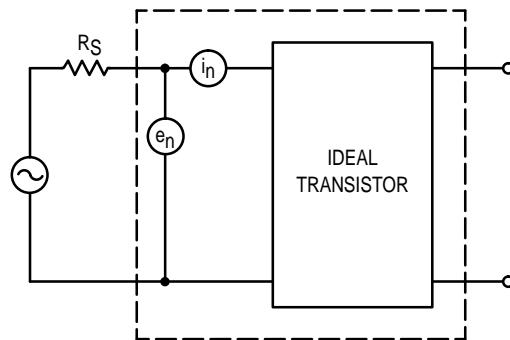
1. Pulse Test: Pulse Width $\leq 2.0\%$.2. $f_T = |h_{fe}| \cdot f_{\text{test}}$ 

Figure 1. Transistor Noise Model