

SANYO

No.676D

2SB808/2SD1012

PNP/NPN Epitaxial Planar Silicon Transistors

Low-Voltage Large-Current
Amp Applications

(): 2SB808

Absolute Maximum Ratings at $T_a=25^\circ\text{C}$

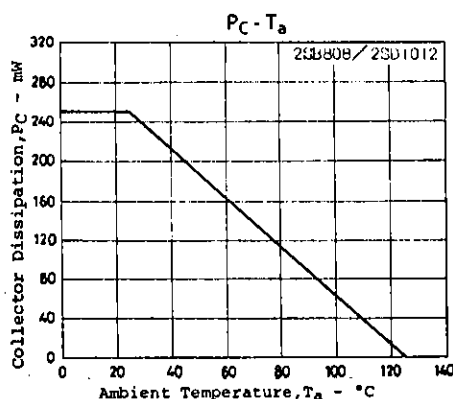
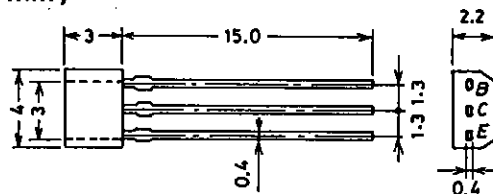
			unit
Collector to Base Voltage	V_{CB0}	(-) 20	V
Collector to Emitter Voltage	V_{CEO}	(-) 15	V
Emitter to Base Voltage	V_{EBO}	(-) 5	V
Collector Current	I_C	(-) 0.7	A
Collector Current(Pulse)	I_{CP}	(-) 1.5	A
Collector Dissipation	P_C	250	mW
Junction Temperature	T_j	125	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +125	$^\circ\text{C}$

Electrical Characteristics at $T_a=25^\circ\text{C}$

			min	typ	max	unit
Collector Cutoff Current	I_{CBO}	$V_{CB}=(-)15\text{V}, I_E=0$		(-) 1.0		μA
Emitter Cutoff Current	I_{EBO}	$V_{EB}=(-)4\text{V}, I_C=0$		(-) 1.0		μA
DC Current Gain	$h_{FE(1)}$	$V_{CE}=(-)2\text{V}, I_C=(-)50\text{mA}$	160*		960*	
	$h_{FE(2)}$	$V_{CE}=(-)2\text{V}, I_C=(-)500\text{mA}$	80			
		Pulse				
Gain-Bandwidth Product	f_T	$V_{CE}=(-)10\text{V}, I_C=(-)50\text{mA}$		250		MHz
Common Base Output Capacitance	C_{ob}	$V_{CB}=(-)10\text{V}, f=1\text{MHz}$		(13)		pF
Collector to Emitter Saturation Voltage	$V_{CE(sat)1}$	$I_C=(-)5\text{mA}, I_E=(-)0.5\text{mA}$	(-) 1.5	(-) 3.5		mV
	$V_{CE(sat)2}$	$I_C=(-)100\text{mA}, I_E=(-)10\text{mA}$	(-) 60	(-) 120		mV
Base to Emitter Saturation Voltage	$V_{BE(sat)}$	$I_C=(-)100\text{mA}, I_E=(-)10\text{mA}$	(-) 0.8	(-) 1.2		V
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C=(-)10\mu\text{A}, I_E=0$	(-) 20			V
Collector to Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C=(-)1\text{mA}, R_{BE}=\infty$	(-) 15			V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E=(-)10\mu\text{A}, I_C=0$	(-) 5			V

* The 2SB808/2SD1012 are classified by 50mA h_{FE} as follows :

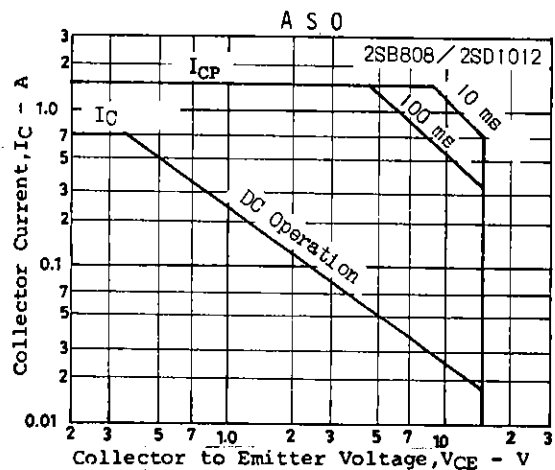
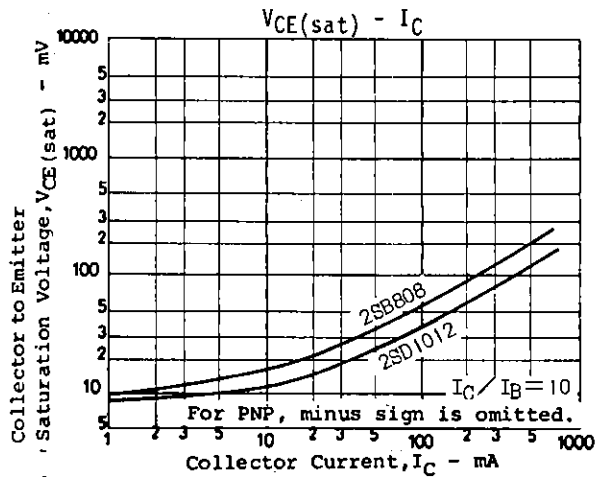
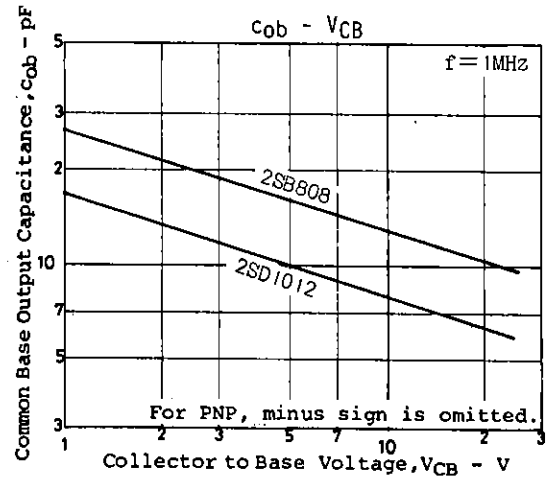
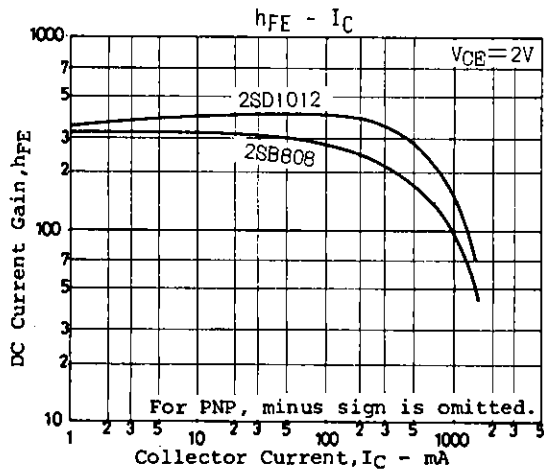
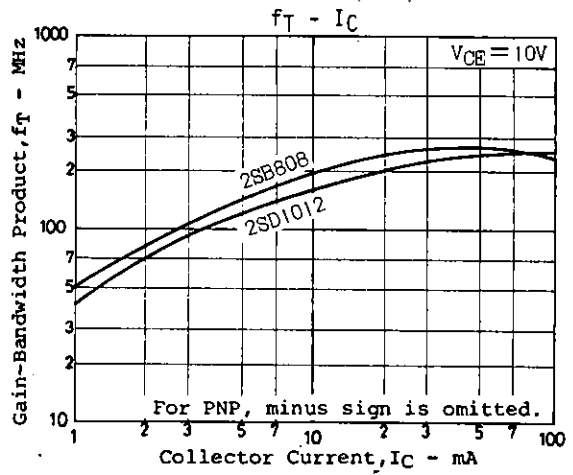
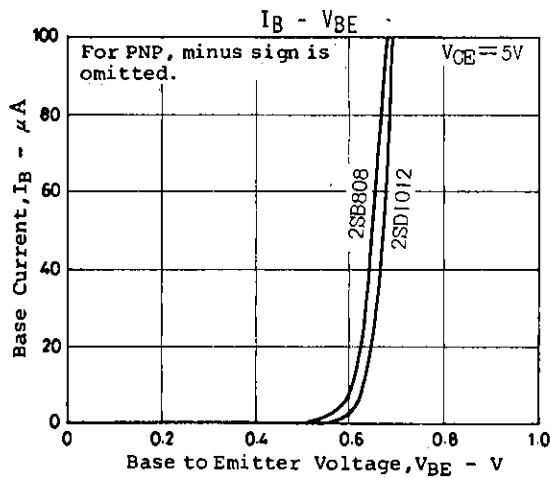
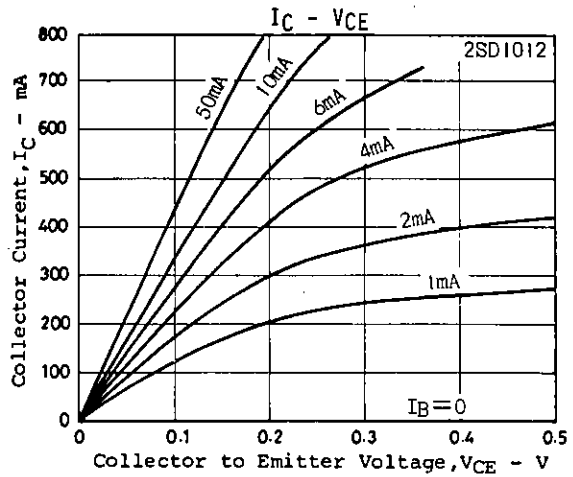
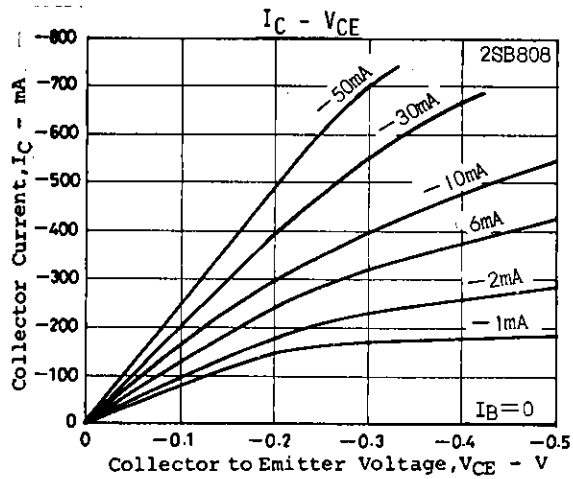
2SB808	160	F	320	280	G	560	
2SD1012	160	F	320	280	G	560	480 H 960

Package Dimensions 2033
(unit: mm)B: Base
C: Collector
E: Emitter

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SANYO Electric Co., Ltd. Semiconductor Business Headquarters

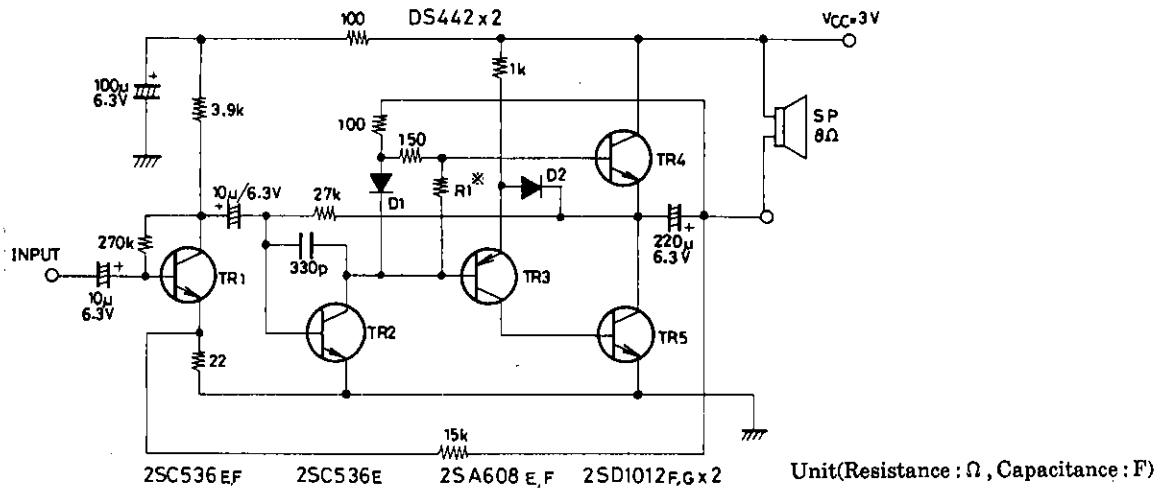
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN



Sample Application Circuit : Low-voltage 3V(P_O 120mW) ITL-OTL power amp.

. Circuit configuration

For obtaining an output of more than 100mW, the middle-point voltage at the output stage and the collector voltage of the driver transistor must be $V_{CC}/2$. Therefore, the output stage is of quasi complementary configuration composed of npn/npn transistors. The phase is reversed by the 2SA608 and the middle-point voltage at the output stage and the collector voltage of the driver transistor are made to be $V_{CC}/2$ so that the output can be maximized.

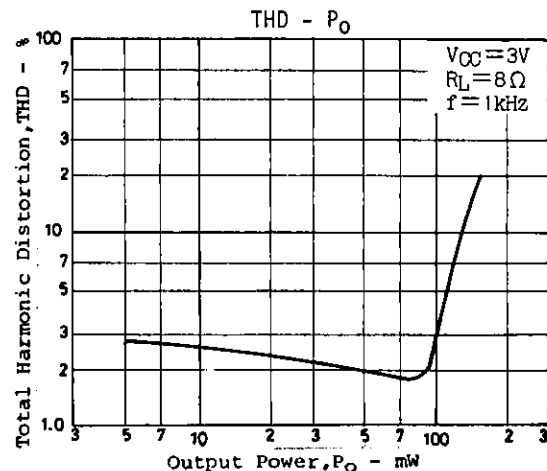
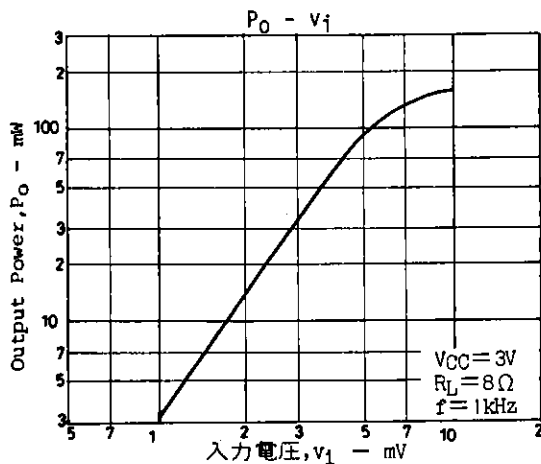


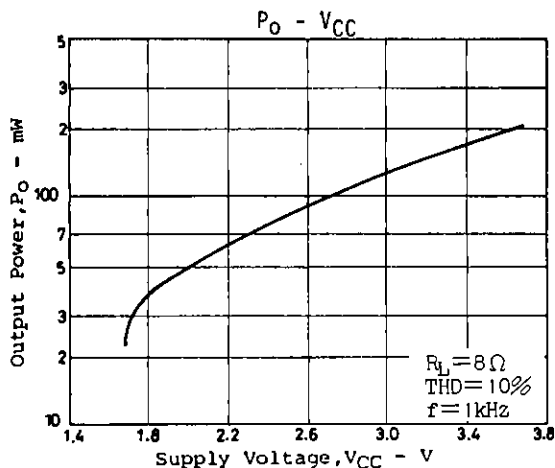
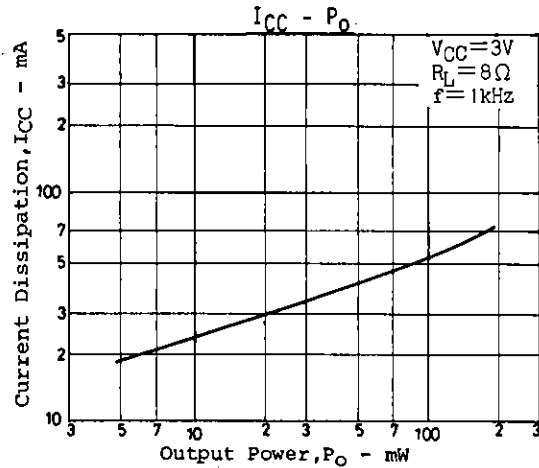
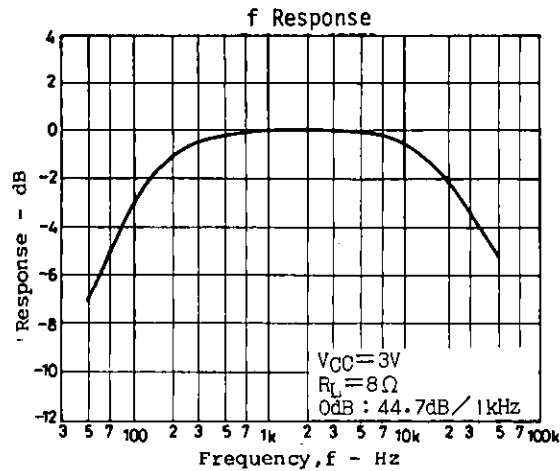
R_1 : Used control idle current
 For $R_1 = 820\Omega$, use rank F for [TR4,5(2SD1012)].
 For $R_1 = 680\Omega$, use rank G for [TR4,5(2SD1012)].

. Main Specifications

Characteristic	Conditions	f=400Hz	f=1kHz	unit
Current dissipation	Quiescent, total current dissipation	11.0 to 15.5	11.0 to 15.5	mA
Output power	THD=10%	120 to 125	127 to 130	mW
Voltage gain	$P_O=10\text{mW}$	43.3 to 45.5	43.5 to 45.7	dB
Total harmonic distortion	$P_O=50\text{mW}$	1.4 to 2.6	1.3 to 2.5	%
Input resistance	$P_O=10\text{mW}$	10.4 to 20.5	11.0 to 21.0	k Ω

Note : For above-mentioned h_{FE} rank.





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