

Silicon NPN Power Transistors

2SD1710

DESCRIPTION

- With TO-3PML package
- High voltage;high speed
- High reliability.

APPLICATIONS

- Ultrahigh-definition CRT display
- Horizontal deflection output applications

PINNING

PIN	DESCRIPTION
1	Base
2	Collector
3	Emitter

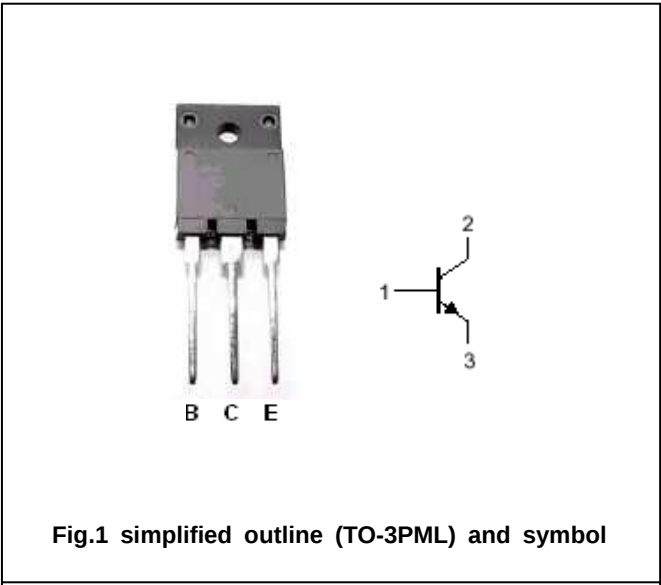


Fig.1 simplified outline (TO-3PML) and symbol

Absolute maximum ratings(Ta=25℃)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	1500	V
V_{CEO}	Collector-emitter voltage	Open base	800	V
V_{EBO}	Emitter-base voltage	Open collector	6	V
I_C	Collector current		5	A
P_C	Collector power dissipation	$T_C=25^{\circ}C$	50	W
T_j	Junction temperature		150	℃
T_{stg}	Storage temperature		-55~150	℃

Silicon NPN Power Transistors

2SD1710

CHARACTERISTICS

Tj=25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
$V_{CEO(SUS)}$	Collector-emitter sustaining voltage	$I_C=100mA; I_B=0$	800			V
V_{CEsat}	Collector-emitter saturation voltage	$I_C=4.5A; I_B=2A$			5.0	V
V_{BEsat}	Base-emitter saturation voltage	$I_C=4.5A; I_B=2A$			1.5	V
I_{EBO}	Emitter cut-off current	$V_{EB}=4V; I_C=0$			0.1	mA
I_{CBO}	Collector cut-off current	$V_{CB}=800V; I_E=0$			10	μA
I_{CES}	Collector cut-off current	$V_{CE}=1500V; R_{BE}=0$			1.0	mA
h_{FE}	DC current gain	$I_C=0.5 A; V_{CE}=5V$	10		40	

Silicon NPN Power Transistors

2SD1710

PACKAGE OUTLINE

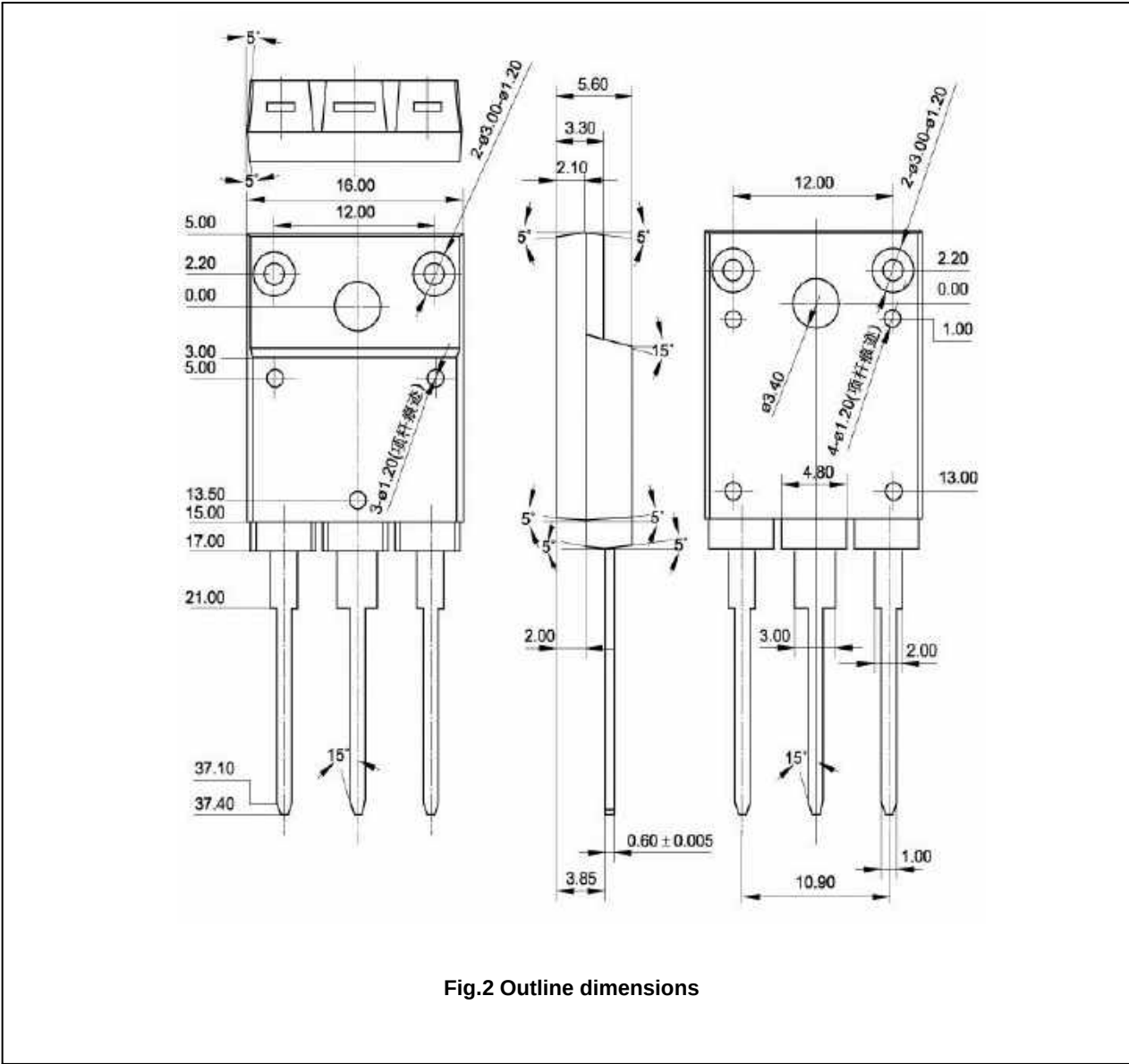


Fig.2 Outline dimensions