

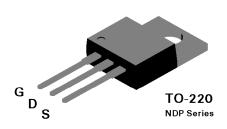
NDP6020 / NDB6020 N-Channel Logic Level Enhancement Mode Field Effect Transistor

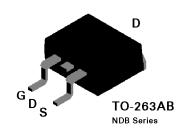
General Description

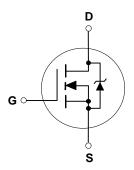
These logic level N-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as automotive, DC/DC converters, PWM motor controls, and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- Critical DC electrical parameters specified at elevated temperature.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- 175°C maximum junction temperature rating.
- High density cell design for extremely low R_{DS(ON)}.
- TO-220 and TO-263 (D²PAK) package for both through hole and surface mount applications.







Absolute Maximum Ratings T_o = 25°C unless otherwise noted

Symbol	Parameter	NDP6020	NDB6020	Units	
V _{DSS}	Drain-Source Voltage		V		
V_{DGR}	Drain-Gate Voltage ($R_{GS} \le 1 \text{ M}\Omega$)		V		
V _{GSS}	Gate-Source Voltage - Continuous	±8			
I _D	Drain Current - Continuous	;	Α		
	- Pulsed	1	00		
P _D	Total Power Dissipation @ T _C = 25°C		60		
	Derate above 25°C		0.4	W/°C	
T _J ,T _{STG}	Operating and Storage Temperature Range	-65	to 175	°C	

Symbol	Parameter	Conditions		Min	Тур	Max	Units
OFF CH	ARACTERISTICS			•			
3V _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_{D} = 250 \mu\text{A}$		20			V
DSS	Zero Gate Voltage Drain Current	V _{DS} = 16 V, V _{GS} = 0 V				1	μΑ
			$T_J = 55^{\circ}C$			10	mA
GSSF	Gate - Body Leakage, Forward	$V_{GS} = 8 \text{ V}, V_{DS} = 0 \text{ V}$	•			100	nA
GSSR	Gate - Body Leakage, Reverse	$V_{GS} = -8 \text{ V}, V_{DS} = 0 \text{ V}$				-100	nA
ON CHAI	RACTERISTICS (Note 1)						
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$		0.4	0.62	1	V
			$T_J = 125^{\circ}C$	0.2	0.35	0.7	
R _{DS(ON)}	Static Drain-Source On-Resistance	$V_{GS} = 4.5 \text{ V}, I_{D} = 18 \text{ A}$			0.019	0.023	Ω
			$T_{J} = 125^{\circ}C$		0.024	0.032	
		$V_{GS} = 2.7 \text{ V}, I_{D} = 16 \text{ A}$			0.024	0.028	
D(on)	On-State Drain Current	$V_{GS} = 4.5 \text{ V}, V_{DS} = 5 \text{ V}$		60			Α
FS	Forward Transconductance	$V_{DS} = 5 \text{ V}, I_{D} = 18 \text{ A}$			29		S
OYNAMIC	CHARACTERISTICS					1	
Ciss	Input Capacitance	$V_{DS} = 10 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1.0 MHz			1170		pF
Coss	Output Capacitance				610		pF
C _{rss}	Reverse Transfer Capacitance				180		pF
WITCH	NG CHARACTERISTICS (Note 1)						
D(on)	Turn - On Delay Time	$V_{DD} = 20 \text{ V}, I_D = 35 \text{ A},$			7	20	nS
r	Turn - On Rise Time	$V_{GS} = 5 \text{ V, } R_{GEN} = 10 \Omega$ $R_L = 0.5 \Omega$			148	300	nS
D(off)	Turn - Off Delay Time				98	200	nS
	Turn - Off Fall Time				233	450	nS
\mathbf{Q}_{g}	Total Gate Charge	$V_{DS} = 15 \text{ V},$ $I_{D} = 35 \text{ A}, V_{GS} = 5 \text{ V}$			32	45	nC
Q_{gs}	Gate-Source Charge	$I_D = 35 \text{ A}, \ V_{GS} = 5 \text{ V}$			6		nC
Q_{gd}	Gate-Drain Charge				11		nC

Symbol	Parameter	Min	Тур	Max	Units	
DRAIN-S	OURCE DIODE CHARACTERISTICS	•	·			
I _s	Maximum Continuous Drain-Source Dioc			35	Α	
I _{SM}	Maximum Pulsed Drain-Source Diode Fo			100	Α	
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = 35 \text{ A (Note 1)}$		1.1	1.3	V
t _{rr}	Reverse Recovery Time	$V_{GS} = 0 \text{ V}, I_F = 35 \text{ A},$ $dI_F/dt = 100 \text{ A/}\mu\text{s}$		43	90	ns
I _{rr}	Reverse Recovery Current	$u_{F}/ut = 100 \text{ AV}\mu\text{S}$		1.1	3	Α
THERMA	L CHARACTERISTICS	•	·			
R _{eJC}	Thermal Resistance, Junction-to-Case			2.5	°C/W	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambier			62.5	°C/W	

Note: 1. Pulse Test: Pulse Width \leq 300 µs, Duty Cycle \leq 2.0%.

Typical Electrical Characteristics

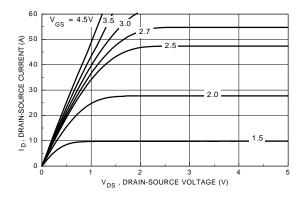
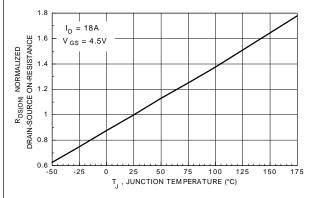


Figure 1. On-Region Characteristics.

Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.



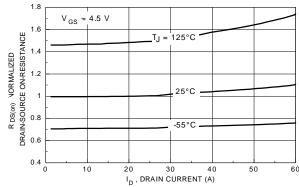
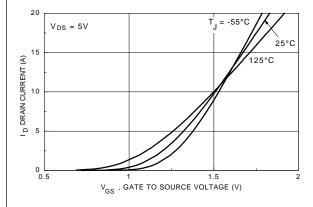


Figure 3. On-Resistance Variation with Temperature.

Figure 4. On-Resistance Variation with Drain Current and Temperature.



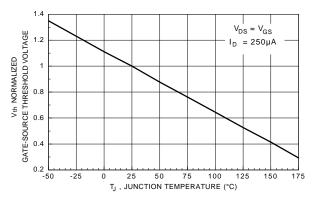


Figure 5. Transfer Characteristics.

Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics (continued)

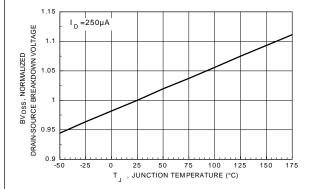


Figure 7. Breakdown Voltage Variation with Temperature.

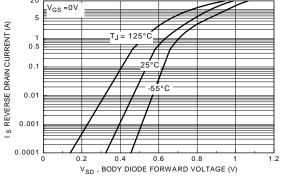


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature.

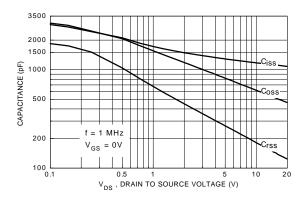


Figure 9. Capacitance Characteristics.

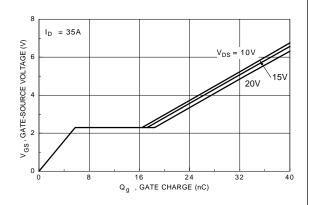


Figure 10. Gate Charge Characteristics.

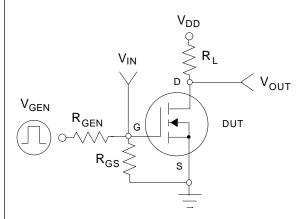


Figure 11. Switching Test Circuit.

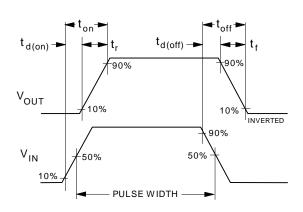
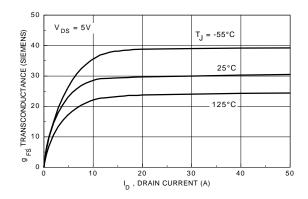


Figure 12. Switching Waveforms.

Typical Electrical Characteristics (continued)



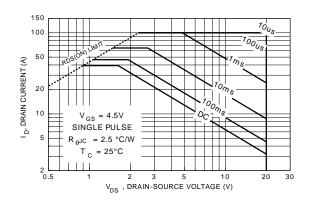


Figure 13. Transconductance Variation with Drain Current and Temperature.

Figure 14. Maximum Safe Operating Area.

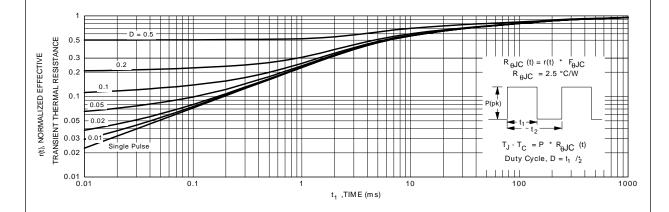
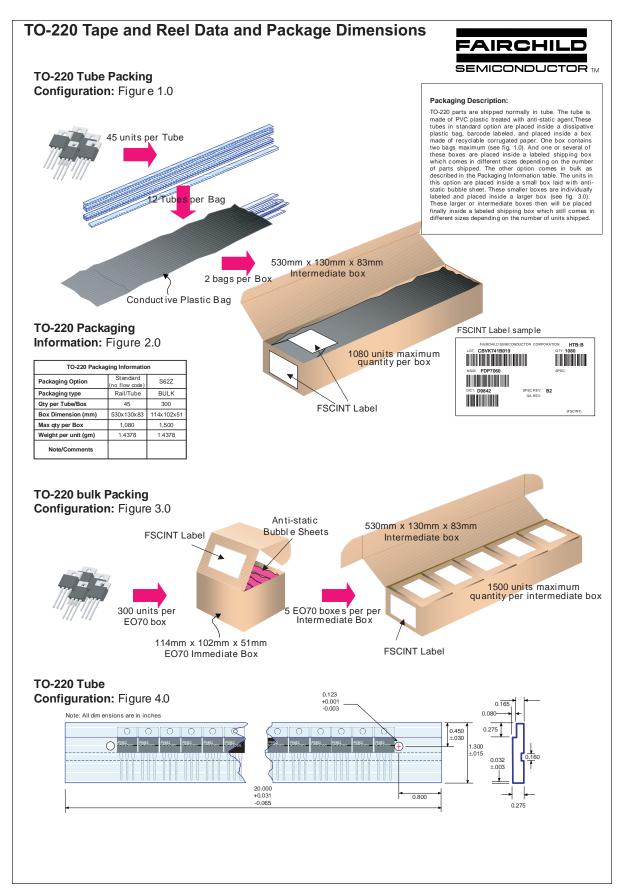
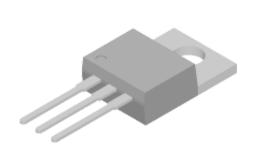


Figure 15. Transient Thermal Response Curve.

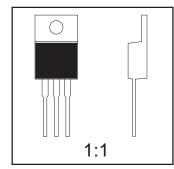


TO-220 Tape and Reel Data and Package Dimensions, continued

TO-220 (FS PKG Code 37)

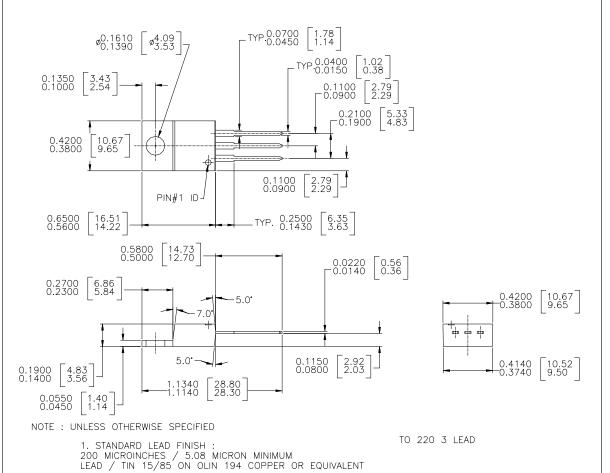


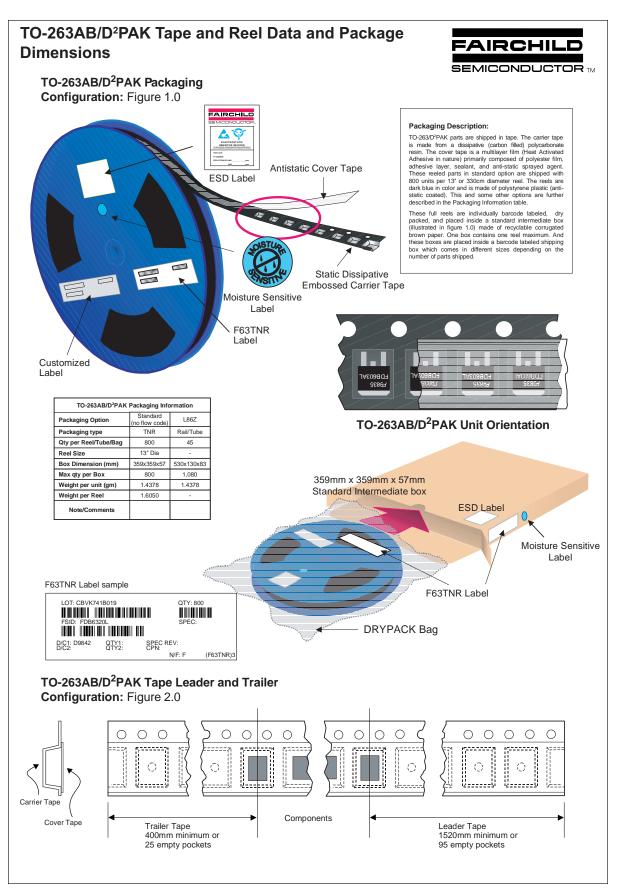
2. DIMENSION BASED ON JEDEC STANDARD TO-220 VARIATION AB, ISSUE J, DATED 3/24/87



Scale 1:1 on letter size paper
Dimensions shown below are in:
inches [millimeters]

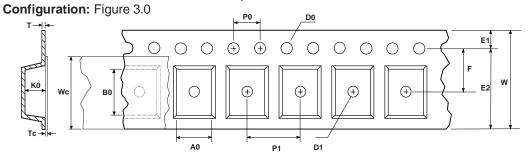
Part Weight per unit (gram): 1.4378





TO-263AB/D²PAK Tape and Reel Data and Package Dimensions, continued

TO-263AB/D²PAK Embossed Carrier Tape



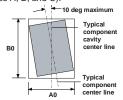
User Direction of Feed

Dimensions are in millimeter														
Pkg type	Α0	В0	w	D0	D1	E1	E2	F	P1	P0	K0	Т	Wc	Тс
TO263AB/ D ² PAK (24mm)	10.60 +/-0.10	15.80 +/-0.10	24.0 +/-0.3	1.55 +/-0.05	1.60 +/-0.10	1.75 +/-0.10	22.25 min	11.50 +/-0.10	16.0 +/-0.1	4.0 +/-0.1	4.90 +/-0.10	0.450 +/-0.150	21.0 +/-0.3	0.06 +/-0.02

Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



Sketch A (Side or Front Sectional View)
Component Rotation

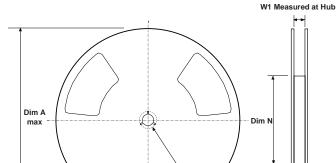


Sketch B (Top View)
Component Rotation

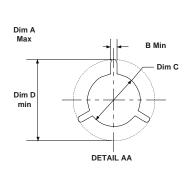


Sketch C (Top View)
Component lateral movement

TO-263AB/D²PAK Reel Configuration: Figure 4.0







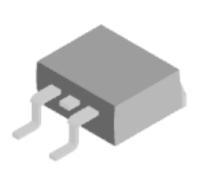
W2 max Measured at Hub

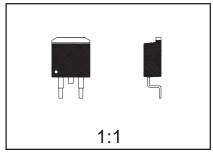
See detail AA

Dimensions are in inches and millimeters									
Tape Size	Reel Option	Dim A	Dim B	Dim C	Dim D	Dim N	Dim W1	Dim W2	Dim W3 (LSL-USL)
24mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	4.00 100	0.961 +0.078/-0.000 24.4 +2/0	1.197 30.4	0.941 - 0.1.079 23.9 - 27.4

TO-263AB/D²PAK Tape and Reel Data and Package Dimensions, continued

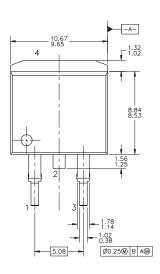
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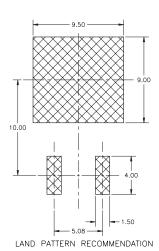


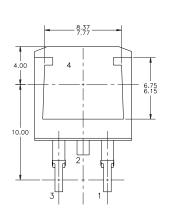


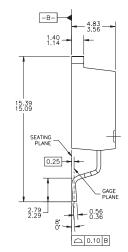
Scale 1:1 on letter size paper Dimensions shown below are in: inches [millimeters]

Part Weight per unit (gram): 1.4378









- NOTES: UNLESS OTHERWISE SPECIFIED

 A) ALL DIMENSIONS ARE IN MILLIMETERS.
 B) STANDARD LEAD FINISH:
 200 MICROINCHES / 5.08 MICROMETERS MIN.
 LEAD/TIN 15/85 ON OLIN 194 COPPER OR
 EQUIVALENT.
 C) MAXIMUM YERTICAL BURR ON HEATSINK NOT
 TO EXCEED 0.003 INCH / 0.05mm.
 D) NO PACKAGE CHIPS, CRACKS OR SURFACE
 IDENTIFICATION ALLOWED AFTER FORMING.
 E) REFERENCE JEDEC, TO—265, ISSUE C,
 VARIATION AB, DATED 2/92.

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