

TrenchMOS™ transistor

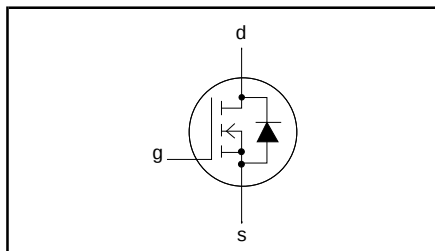
Logic level FET

PHP45N03LT

FEATURES

- 'Trench' technology
- Very low on-state resistance
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

$$V_{DSS} = 30 \text{ V}$$

$$I_D = 45 \text{ A}$$

$$R_{DS(ON)} \leq 24 \text{ m}\Omega \text{ (} V_{GS} = 5 \text{ V)}$$

$$R_{DS(ON)} \leq 21 \text{ m}\Omega \text{ (} V_{GS} = 10 \text{ V)}$$

GENERAL DESCRIPTION

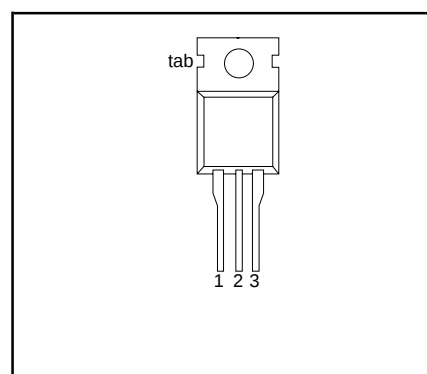
N-channel enhancement mode logic level field-effect power transistor in a plastic envelope using 'trench' technology. The device has very low on-state resistance. It is intended for use in dc to dc converters and general purpose switching applications.

The PHP45N03LT is supplied in the SOT78 (TO220AB) conventional leaded package.

PINNING

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

SOT78 (TO220AB)



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	30	V
V_{DGR}	Drain-gate voltage	$R_{GS} = 20 \text{ k}\Omega$	-	30	V
$\pm V_{GS}$	Gate-source voltage	-	-	15	V
I_D	Drain current (DC)	$T_{mb} = 25 \text{ }^\circ\text{C}$	-	45	A
I_D	Drain current (DC)	$T_{mb} = 100 \text{ }^\circ\text{C}$	-	36	A
I_{DM}	Drain current (pulse peak value)	$T_{mb} = 25 \text{ }^\circ\text{C}$	-	180	A
P_{tot}	Total power dissipation	$T_{mb} = 25 \text{ }^\circ\text{C}$	-	86	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	$^\circ\text{C}$

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\text{-}j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	1.75	K/W
$R_{th\text{-}j\text{-}a}$	Thermal resistance junction to ambient	in free air	60	-	K/W

TrenchMOS™ transistor

Logic level FET

PHP45N03LT

STATIC CHARACTERISTICS

 $T_j = 25^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 0.25\text{ mA}; T_j = -55^\circ\text{C}$	30	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}; I_D = 1\text{ mA}; T_j = -55^\circ\text{C}$	27	-	-	V
		$T_j = 175^\circ\text{C}$	1	1.5	2	V
		$T_j = -55^\circ\text{C}$	0.5	-	-	V
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 30\text{ V}; V_{GS} = 0\text{ V}; T_j = 175^\circ\text{C}$	-	-	2.3	μA
I_{GSS}	Gate source leakage current	$V_{GS} = \pm 5\text{ V}; V_{DS} = 0\text{ V}$	-	0.05	10	μA
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = 5\text{ V}; I_D = 25\text{ A}$	-	-	500	μA
		$V_{GS} = 10\text{ V}; I_D = 25\text{ A}$	-	10	100	nA
		$V_{GS} = 5\text{ V}; I_D = 25\text{ A}; T_j = 175^\circ\text{C}$	-	20	24	m Ω
			-	16	21	m Ω
			-	-	45	m Ω

DYNAMIC CHARACTERISTICS

 $T_j = 25^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	$V_{DS} = 25\text{ V}; I_D = 25\text{ A}$	8	16	-	S
$Q_{g(tot)}$	Total gate charge	$I_D = 40\text{ A}; V_{DD} = 24\text{ V}; V_{GS} = 5\text{ V}$	-	23	-	nC
Q_{gs}	Gate-source charge		-	3	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	12	-	nC
C_{iss}	Input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; f = 1\text{ MHz}$	-	2000	2500	pF
C_{oss}	Output capacitance		-	380	450	pF
C_{rss}	Feedback capacitance		-	250	300	pF
$t_{d on}$	Turn-on delay time	$V_{DD} = 15\text{ V}; I_D = 25\text{ A}; V_{GS} = 5\text{ V}; R_G = 5\text{ }\Omega$	-	30	45	ns
t_r	Turn-on rise time		-	80	130	ns
$t_{d off}$	Turn-off delay time	Resistive load	-	95	135	ns
t_f	Turn-off fall time		-	40	55	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

 $T_j = 25^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	45	A
I_{DRM}	Pulsed reverse drain current		-	-	180	A
V_{SD}	Diode forward voltage	$I_F = 25\text{ A}; V_{GS} = 0\text{ V}$	-	0.95	1.2	V
		$I_F = 40\text{ A}; V_{GS} = 0\text{ V}$	-	1.0	-	V
t_{rr}	Reverse recovery time	$I_F = 40\text{ A}; -dI_F/dt = 100\text{ A}/\mu\text{s}; V_{GS} = -10\text{ V}; V_R = 25\text{ V}$	-	52	-	ns
Q_{rr}	Reverse recovery charge		-	0.08	-	μC

TrenchMOS™ transistor
Logic level FET

PHP45N03LT**AVALANCHE LIMITING VALUE**

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	$I_D = 25\text{ A}$; $V_{DD} \leq 25\text{ V}$; $V_{GS} = 10\text{ V}$; $R_{GS} = 50\ \Omega$; $T_{mb} = 25\text{ °C}$	-	-	60	mJ

TrenchMOS™ transistor

Logic level FET

PHP45N03LT

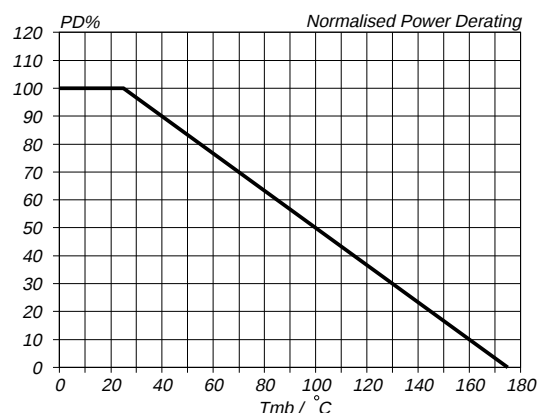


Fig.1. Normalised power dissipation.
 $PD\% = 100 \cdot P_D / P_{D\ 25\ ^\circ C} = f(T_{mb})$

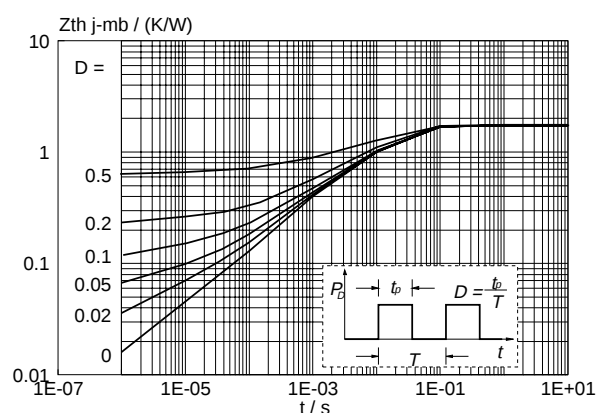


Fig.4. Transient thermal impedance.
 $Z_{th\ j-mb} = f(t)$; parameter $D = t_p / T$

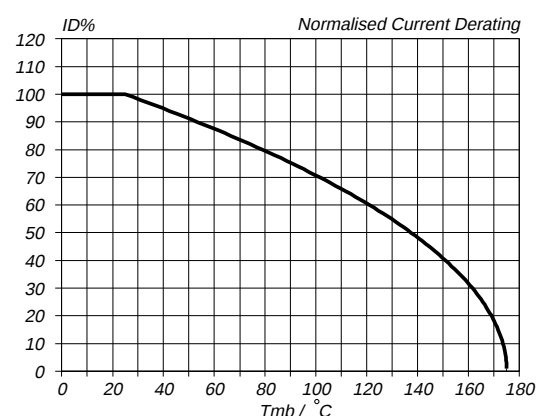


Fig.2. Normalised continuous drain current.
 $ID\% = 100 \cdot I_D / I_{D\ 25\ ^\circ C} = f(T_{mb})$; conditions: $V_{GS} \geq 5\ V$

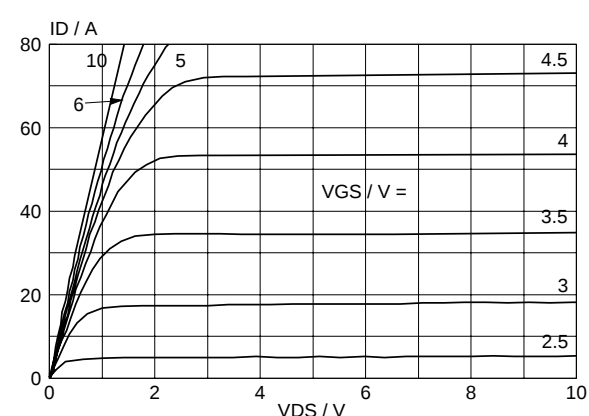


Fig.5. Typical output characteristics, $T_j = 25\ ^\circ C$.
 $I_D = f(V_{DS})$; parameter V_{GS}

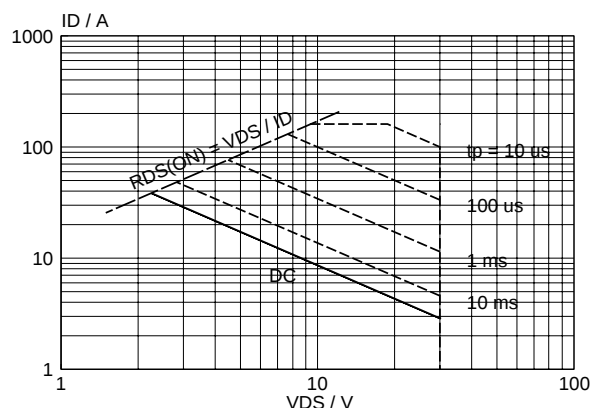


Fig.3. Safe operating area. $T_{mb} = 25\ ^\circ C$
 I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

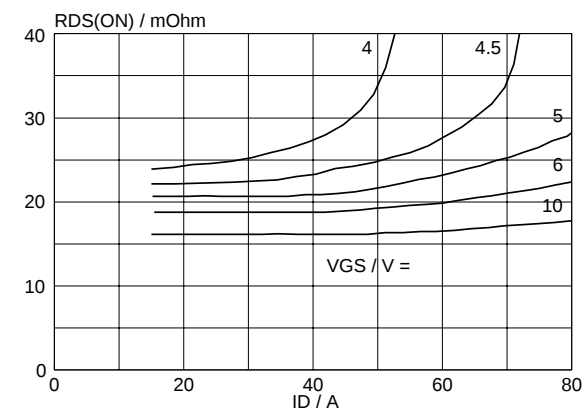
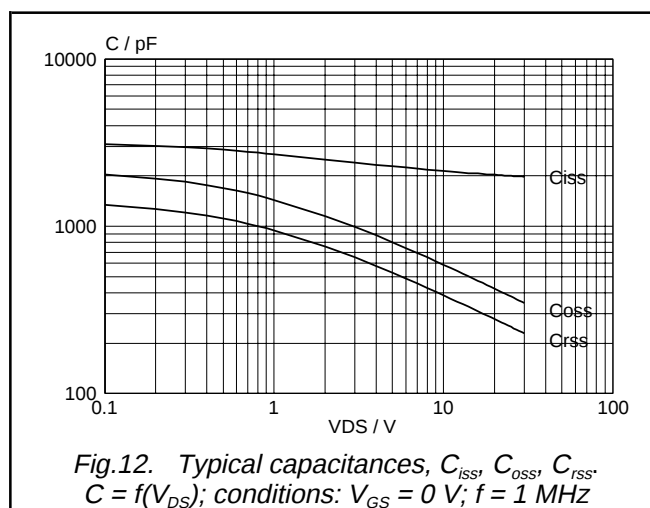
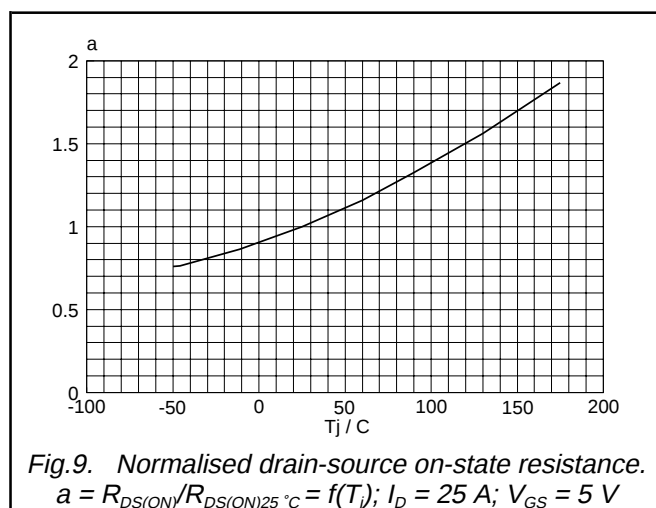
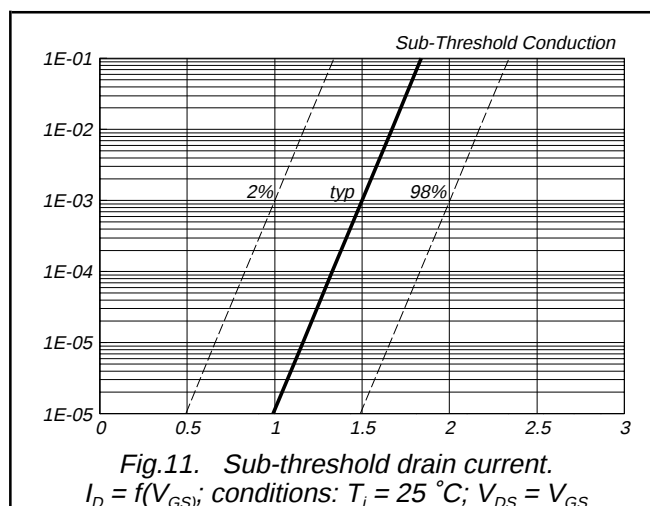
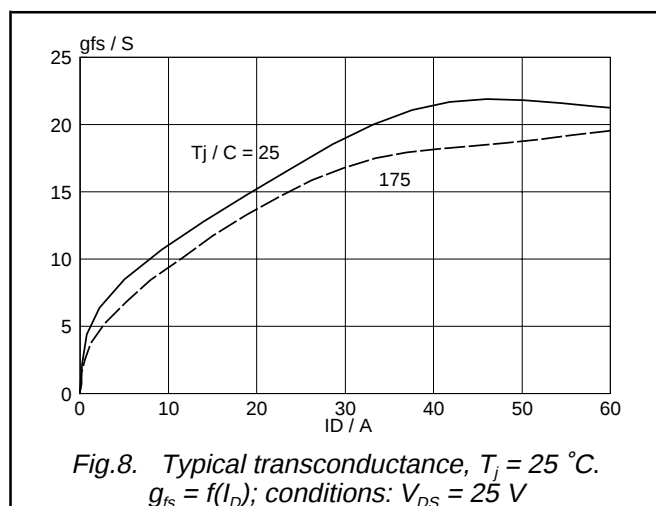
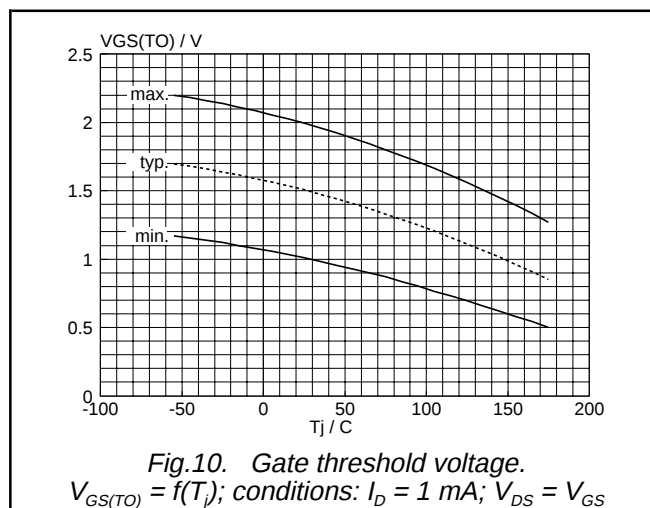
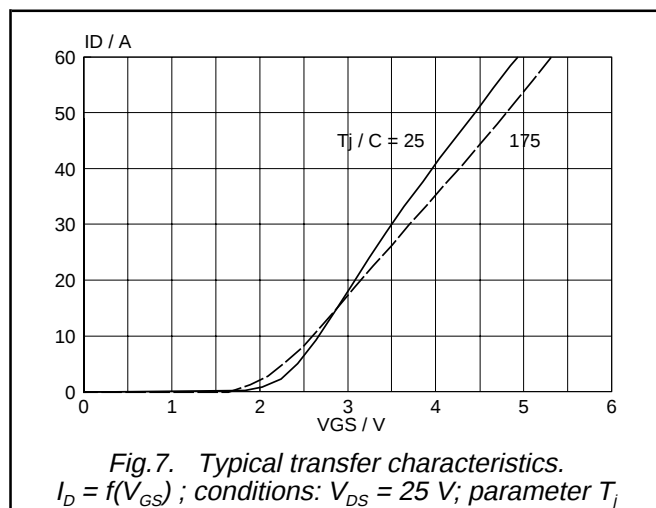


Fig.6. Typical on-state resistance, $T_j = 25\ ^\circ C$.
 $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

TrenchMOS™ transistor

Logic level FET

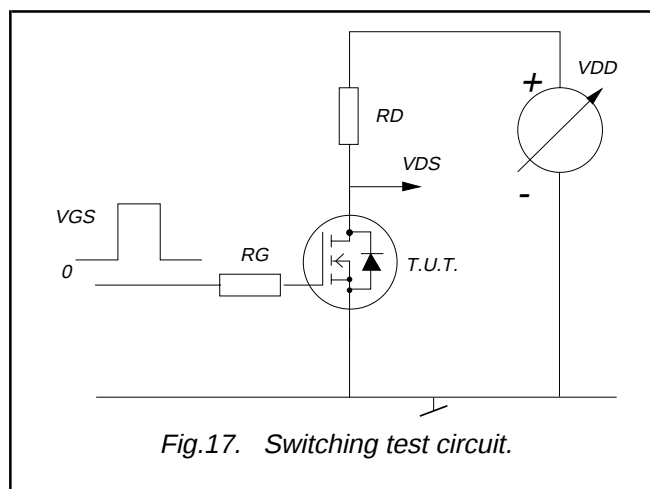
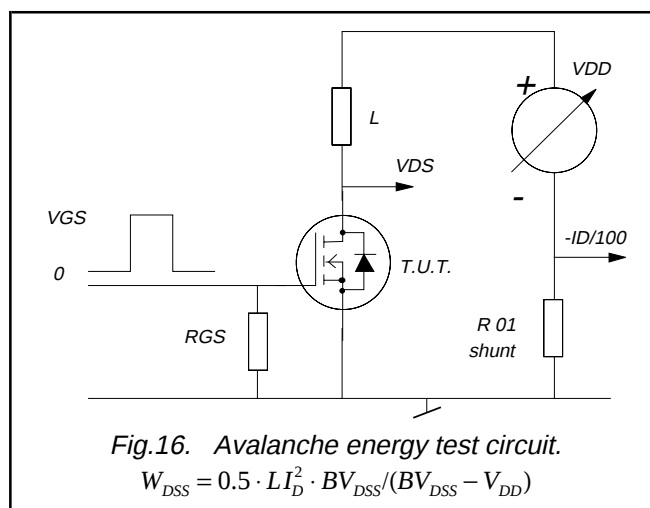
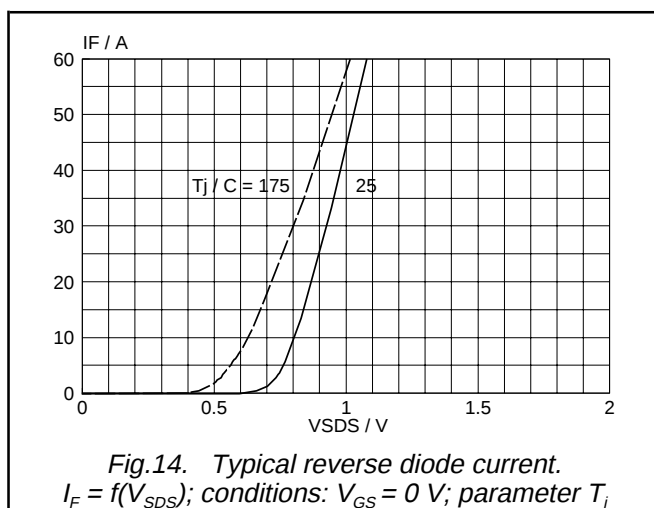
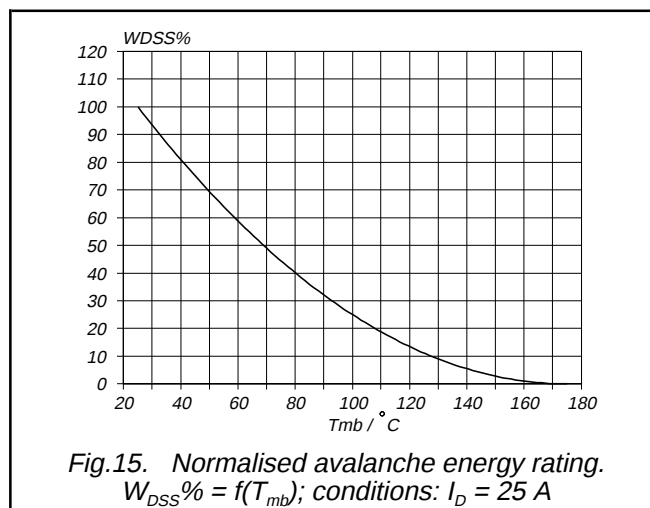
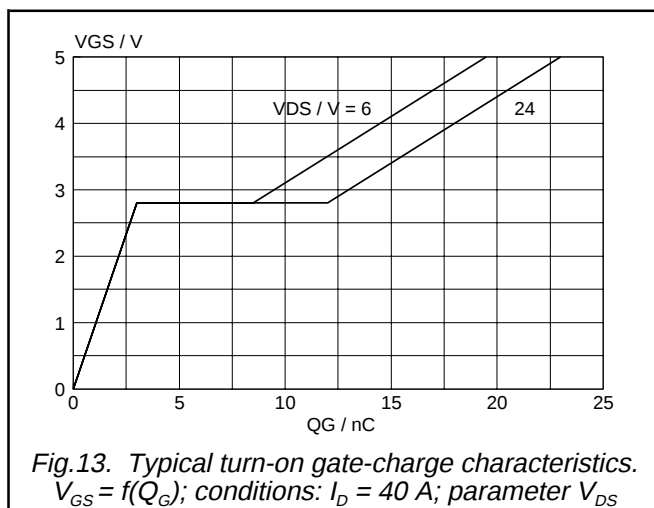
PHP45N03LT



TrenchMOS™ transistor

Logic level FET

PHP45N03LT



TrenchMOS™ transistor

Logic level FET

PHP45N03LT

MECHANICAL DATA

Dimensions in mm

Net Mass: 2 g

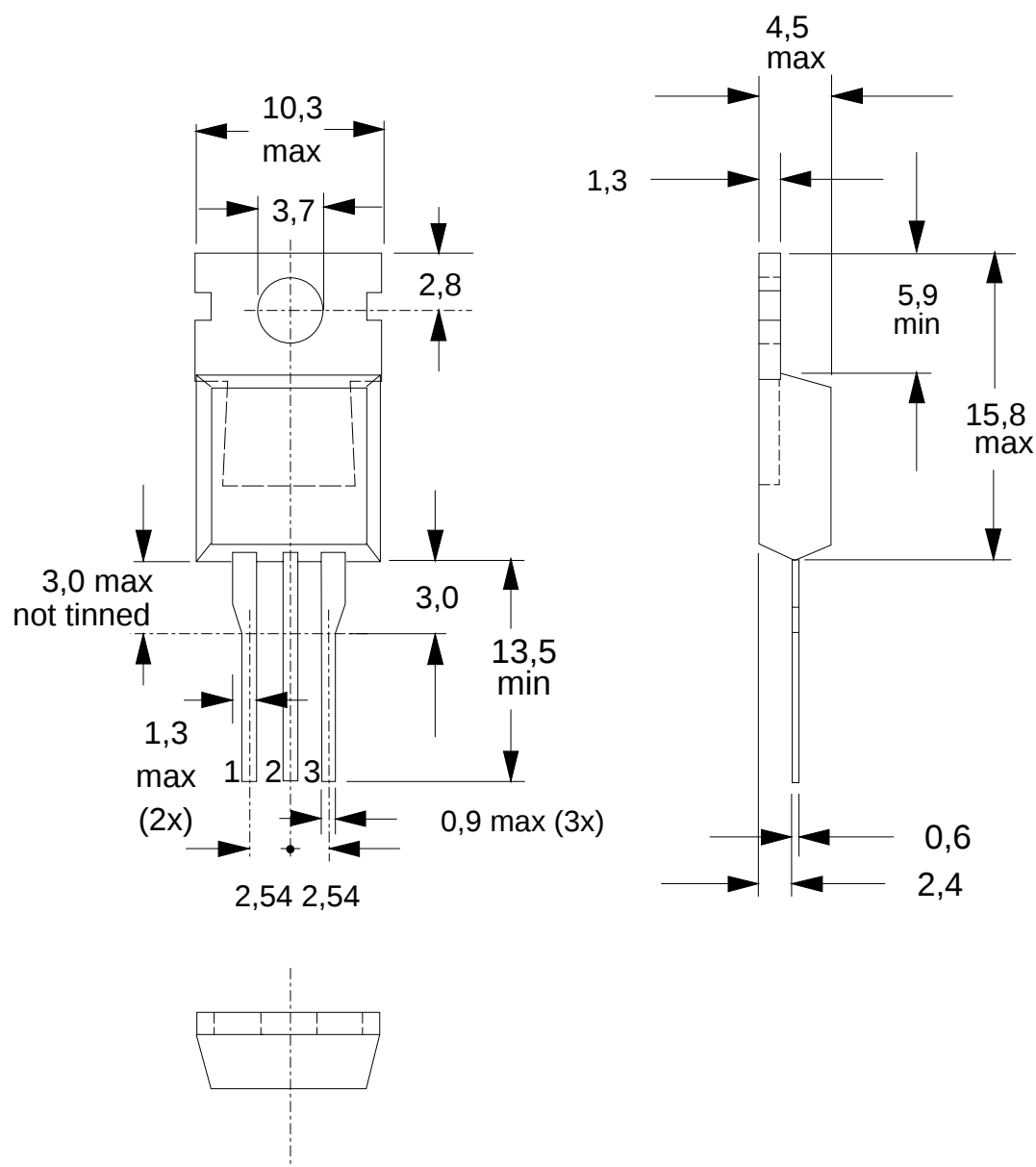


Fig.18. SOT78 (TO220AB); pin 2 connected to mounting base.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Refer to mounting instructions for SOT78 (TO220) envelopes.
3. Epoxy meets UL94 V0 at 1/8".

TrenchMOS™ transistor

Logic level FET

PHP45N03LT

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
© Philips Electronics N.V. 1997	
All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner.	
The information presented in this document does not form part of any quotation or contract, it is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent or other industrial or intellectual property rights.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.