

TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (U-MOS -H)

TK80E07NE

E-Bike/UPS/Inverter

Note : This product is designed for E-Bike / UPS / Inverter in China / India market.

- Low drain-source on-resistance : $R_{DS(ON)} = 6.9 \text{ m}\Omega$ (typ.)
- Low leakage current : $I_{DSS} = 10 \text{ }\mu\text{A}$ (max) ($V_{DS} = 70 \text{ V}$)
- Enhancement mode : $V_{th} = 2.0 \sim 4.0 \text{ V}$ ($V_{DS} = 10 \text{ V}$, $I_D = 0.3 \text{ mA}$)

Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$)

Characteristics	Symbol	Rating	Unit
Drain-source voltage	V_{DSS}	70	V
Drain-gate voltage ($R_{GS} = 20 \text{ k}\Omega$)	V_{DGR}	70	V
Gate-source voltage	V_{GSS}	± 20	V
Drain current	DC (Note 1)	I_D	80
	DC (Note 1,4)	I_D	58
	Pulse (Note 1)	I_{DP}	240
Drain power dissipation ($T_c = 25^\circ\text{C}$)	P_D	87	W
Single pulse avalanche energy (Note 2)	E_{AS}	16.4	mJ
Avalanche current	I_{AR}	40	A
Repetitive avalanche energy (Note 3)	E_{AR}	8.7	mJ
Peak diode recovery dv/dt (Note 5)	dv/dt	11.5	V/ns
Channel temperature (Note 4)	T_{ch}	175	$^\circ\text{C}$
Storage temperature range (Note 4)	T_{stg}	$-55 \sim 175$	$^\circ\text{C}$

Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case	$R_{th(ch-c)}$	1.72	$^\circ\text{C/W}$
Thermal resistance, channel to ambient	$R_{th(ch-a)}$	83.3	$^\circ\text{C/W}$

Note 1: Ensure that the channel temperature does not exceed 175°C .

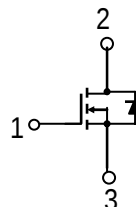
Note 2: $V_{DD} = 25 \text{ V}$, $T_{ch} = 25^\circ\text{C}$ (initial), $L = 14.9 \text{ }\mu\text{H}$, $R_G = 25 \text{ }\Omega$, $I_{AR} = 40 \text{ A}$

Note 3: Repetitive rating: pulse width limited by maximum channel temperature

Note 4: $T_c = 100^\circ\text{C}$

Note 5: $I_{DR} = 80 \text{ A}$, $di/dt = 160 \text{ A}/\mu\text{s}$, $T_{ch} = T_{ch \text{ max.}}$,
 $V_{DS \text{ peak}} < V_{DSS}$

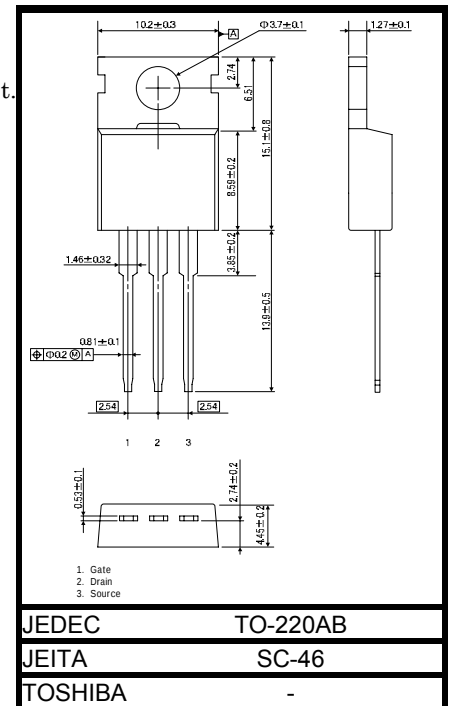
This transistor is an electrostatic-sensitive device.
Please handle with caution.



Note :Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

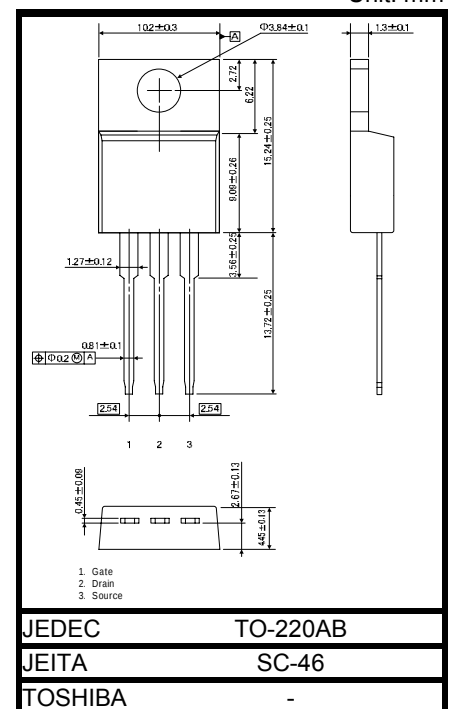
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).Thermal Characteristics

Unit: mm



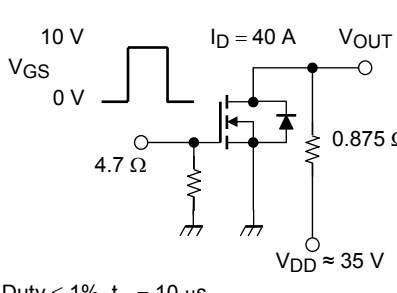
Weight: 1.93g (typ)

Unit: mm



Weight: 1.9 g (typ.)

Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	—	—	± 1	μA
Drain cut-off current		I_{DSS}	$V_{DS} = 70 \text{ V}, V_{GS} = 0 \text{ V}$	—	—	10	μA
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = 10 \text{ mA}, V_{GS} = 0 \text{ V}$	70	—	—	V	
	$V_{(BR)DSX}$	$I_D = 10 \text{ mA}, V_{GS} = -20 \text{ V}$ (Note 5)	45	—	—	V	
Gate threshold voltage		V_{th}	$V_{DS} = 10 \text{ V}, I_D = 0.3 \text{ mA}$	2.0	—	4.0	V
Drain-source ON resistance		$R_{DS(ON)}$	$V_{GS} = 10 \text{ V}, I_D = 40 \text{ A}$	—	6.9	8.5	m Ω
Input capacitance		C_{iss}	$V_{DS} = 10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	—	2270	—	pF
Reverse transfer capacitance		C_{rss}		—	230	—	
Output capacitance		C_{oss}		—	1390	—	
Switching time	Rise time	t_r		—	12	—	ns
	Turn-on time	t_{on}		—	31	—	
	Fall time	t_f		—	17	—	
	Turn-off time	t_{off}		—	47	—	
Total gate charge (Gate-source plus gate-drain)		Q_g	$V_{DD} \approx 56 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 80 \text{ A}$	—	42	—	nC
Gate-source charge		Q_{gs}		—	28	—	
Gate-drain ("miller") charge		Q_{gd}		—	14	—	

Source-Drain Ratings and Characteristics (Ta = 25°C)

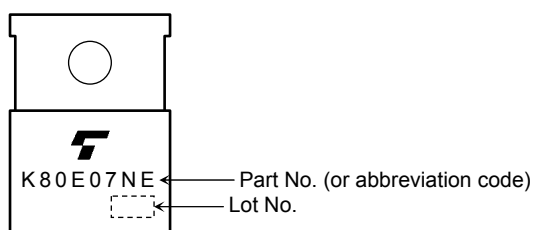
Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Note 1)	I_{DR}	—	—	—	80	A
Pulse drain reverse current (Note 1)	I_{DRP}	—	—	—	240	A
Forward voltage (diode)	V_{DSF}	$I_{DR} = 80 \text{ A}, V_{GS} = 0 \text{ V}$	—	—	-1.5	V
Reverse recovery time (Note 6)	t_{rr}	$I_{DR} = 80 \text{ A}, V_{GS} = 0 \text{ V}$	—	60	—	ns
Reverse recovery charge (Note 6)	Q_{rr}	$dI_{DR}/dt = 50 \text{ A}/\mu\text{s}$	—	45	—	nC

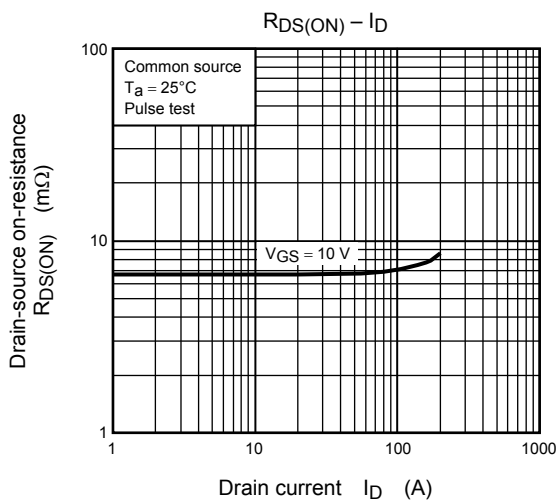
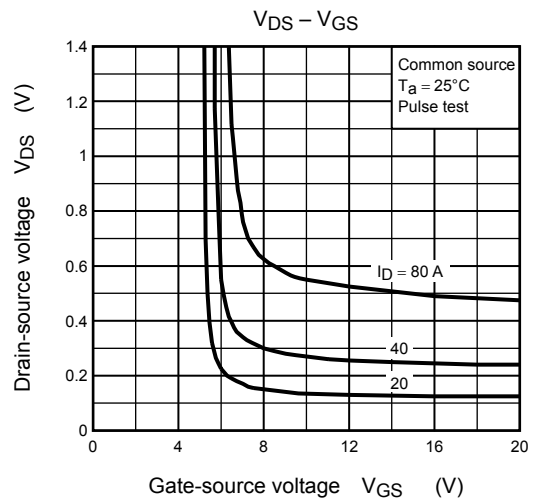
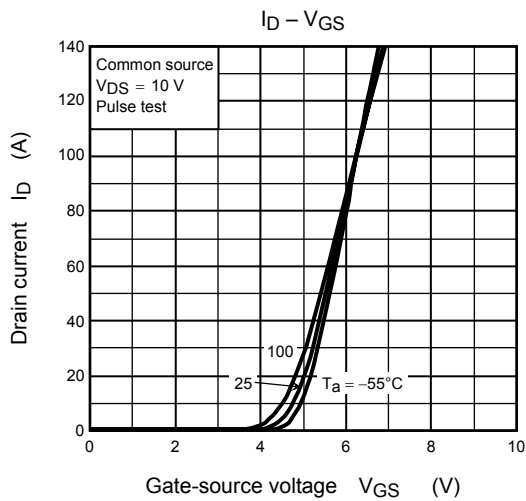
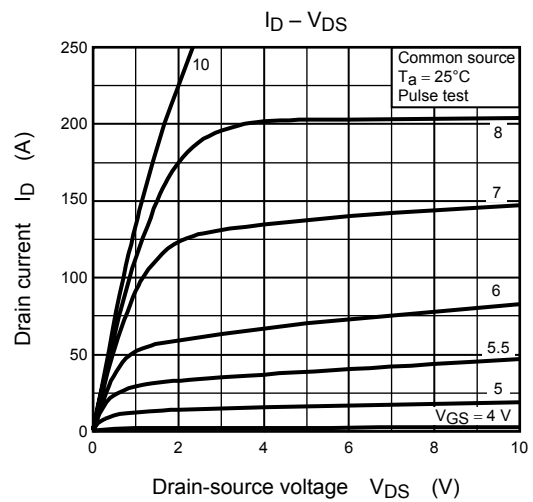
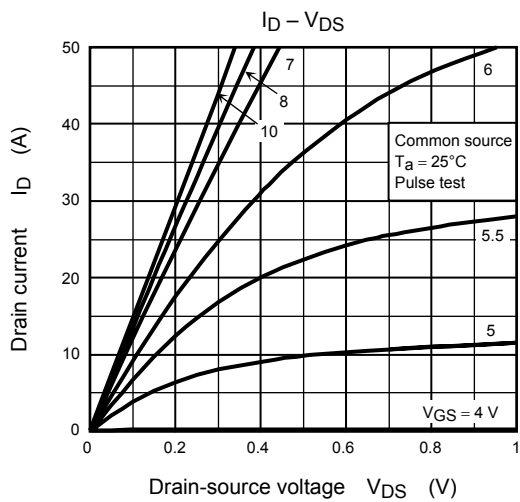
Note 5: If a reverse bias is applied between gate and source, this device enters $V_{(BR)DSX}$ mode.

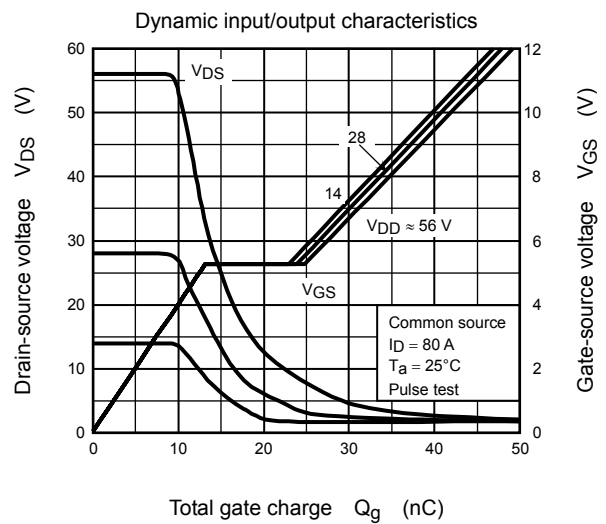
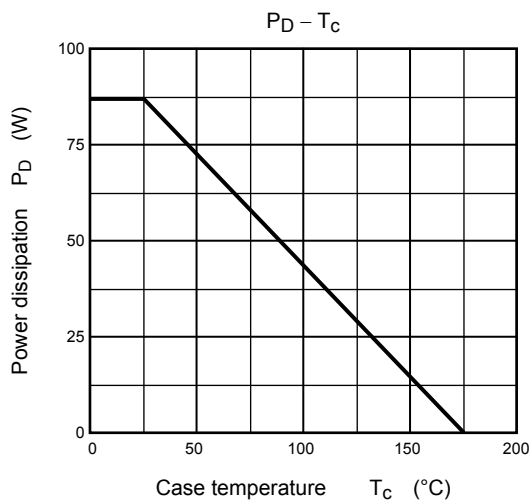
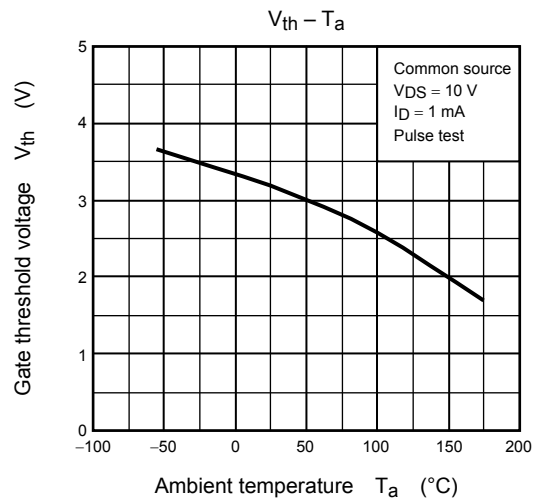
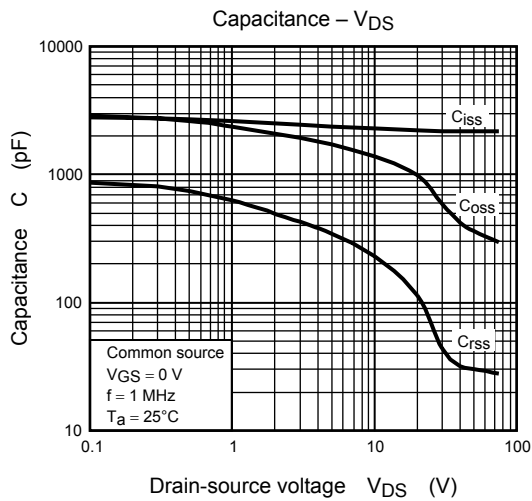
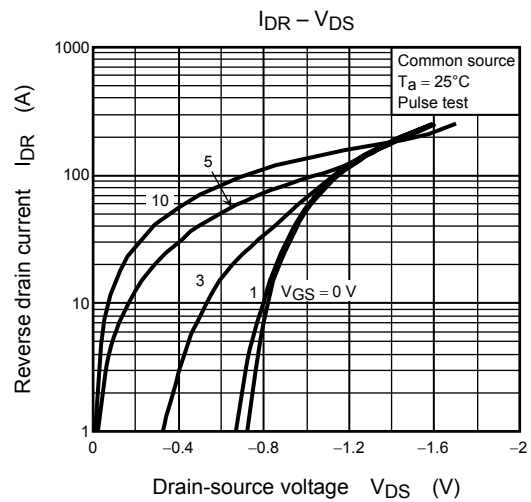
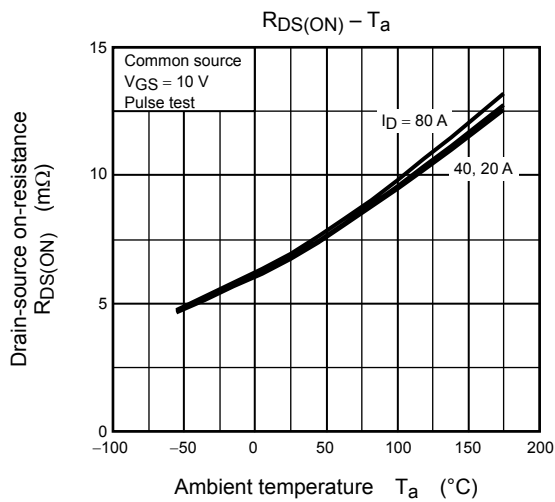
Note that the drain-source breakdown voltage is lowered in this mode.

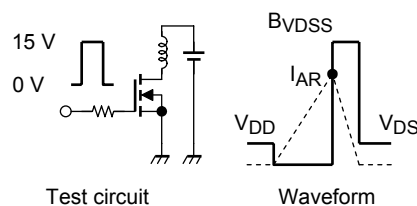
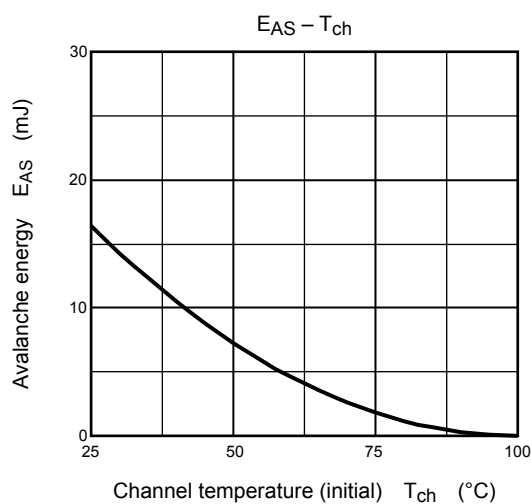
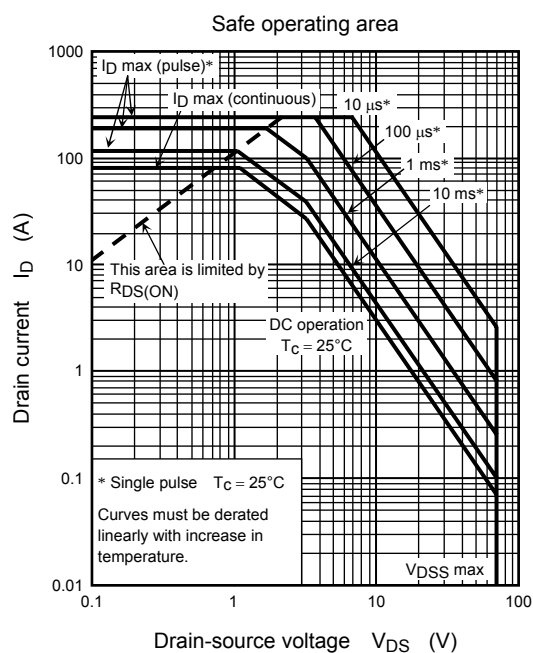
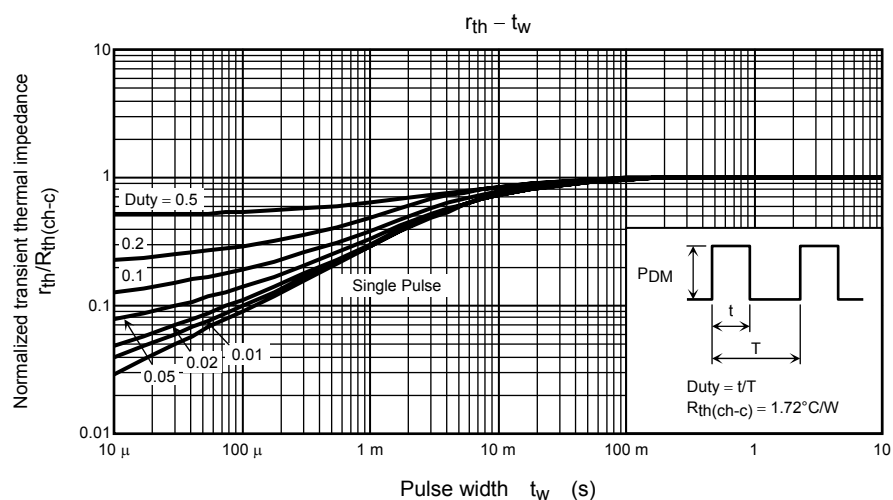
Note 6: Ensure that V_{DS} peak does not exceed V_{DSS} .

Marking









$$R_G = 25 \, \Omega$$

$$V_{DD} = 25 \, \text{V}, L = 14.9 \, \mu\text{H}$$

$$E_{AS} = \frac{1}{2} \cdot L \cdot I_{AR}^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

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