

# 12-bit, serial IN, parallel OUT driver

## BU2090 / BU2090F / BU2090FS / BU2092 / BU2092F / BU2092FV

The BU2090, BU2090F, BU2090FS, BU2092, BU2092F, and BU2092FV are 12-bit serial input, parallel output drivers.

For the BU2090 / F / FS, data input is shifted to the 12-bit internal shift register on the rising edge of a clock pulse. On the falling edge of the pulse, if the DATA pin is HIGH, the data in the shift register is output in parallel to Q0 to Q11.

For the BU2092 / F / FV, shift data read at the rising edge of CLOCK is output in parallel to Q0 to Q11 at the rising edge of LCK. These ICs also have an OE pin, which when HIGH, forces data to be output, regardless of the shift data state.

### ●Applications

Radio cassette players, telephones, compact audio systems, car stereos, and others

### ●Features

- 1) Low power dissipation.
- 2) Operating voltages ranging from 2.7 to 5.5V.
- 3) Output is Nch open drain.
- 4) High output withstand voltage of + 25V.
- 5) Diverse variety of packages.  
BU2090 / F / FS: DIP16, SOP16, SSOP-A16  
BU2092 / F / FV: DIP18, SOP18, SSOP-A18  
(plastic molds)
- 6) High drive capability; direct lighting of green LED possible.

- Absolute maximum ratings (Ta = 25°C)  
(BU2090 / F / FS, BU2092 / F / FV)

| Parameter             |                 | Symbol           | Limits                                        | Unit |
|-----------------------|-----------------|------------------|-----------------------------------------------|------|
| Power supply voltage  |                 | V <sub>DD</sub>  | − 0.3 ~ + 7.0                                 | V    |
| Power dissipation     | BU2090 / F / FS | P <sub>d</sub>   | 1000 (DIP), 300 (SOP), 500 (SSOP)*1           | mW   |
|                       | BU2092 / F / FV |                  | 1050 (DIP), 450 (SOP), 400 (SSOP)*1           |      |
| Power dissipation     | BU2090 / F / FS | P <sub>d</sub>   | 500 (SOP)*2, 650 (SSOP)*3                     | mW   |
|                       | BU2092 / F / FV |                  | 500 (SOP)*2, 650 (SSOP)*4                     |      |
| Operating temperature |                 | T <sub>opr</sub> | − 25 ~ + 75                                   | °C   |
| Storage temperature   |                 | T <sub>stg</sub> | − 55 ~ + 125                                  | °C   |
| Input voltage         |                 | V <sub>IN</sub>  | V <sub>SS</sub> − 0.3 ~ V <sub>DD</sub> + 0.3 | V    |
| Output voltage        |                 | V <sub>O</sub>   | V <sub>SS</sub> ~ 25.0                        | V    |

\*1 Unmounted

\*2 When mounted on a glass epoxy board of 50mm × 50mm × 1.6mm

\*3 When mounted on a glass epoxy board of 90mm × 50mm × 1.6mm

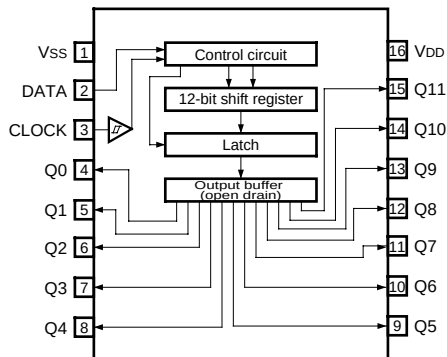
\*4 When mounted on a glass epoxy board of 70mm × 70mm × 1.6mm

- Recommended operating conditions

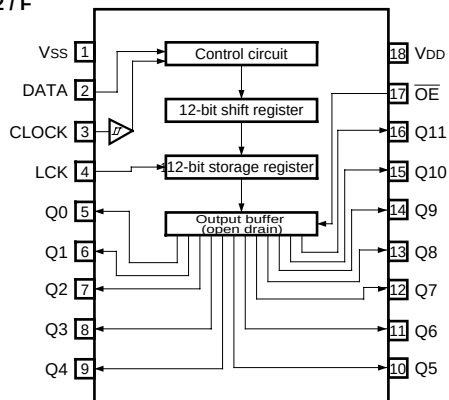
| Parameter            | Symbol          | Limits    | Unit |
|----------------------|-----------------|-----------|------|
| Power supply voltage | V <sub>DD</sub> | 2.7 ~ 5.5 | V    |

## ●Block diagram

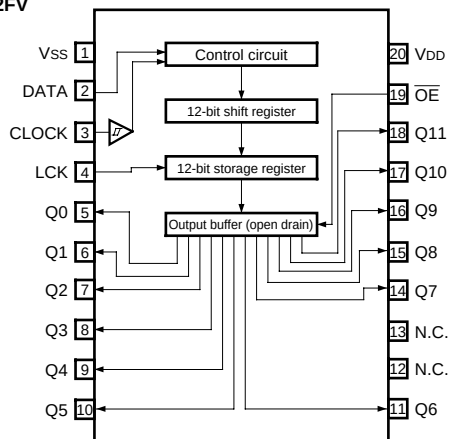
BU2090 / F / FS



BU2092 / F



BU2092FV



## ●Pin descriptions

| Pin No.         |            |             | Pin name               | Function               |
|-----------------|------------|-------------|------------------------|------------------------|
| BU2090 / F / FS | BU2092 / F | BU2092 / FV |                        |                        |
| 1               | 1          | 1           | V <sub>SS</sub>        | GND                    |
| 2               | 2          | 2           | DATA                   | Serial data input      |
| 3               | 3          | 3           | CLOCK                  | Data shift clock input |
| —               | 4          | 4           | LCK                    | Data latch clock input |
| 4               | 5          | 5           | Q0                     | Parallel data output   |
| 5               | 6          | 6           | Q1                     | Parallel data output   |
| 6               | 7          | 7           | Q2                     | Parallel data output   |
| 7               | 8          | 8           | Q3                     | Parallel data output   |
| 8               | 9          | 9           | Q4                     | Parallel data output   |
| 9               | 10         | 10          | Q5                     | Parallel data output   |
| 10              | 11         | 11          | Q6                     | Parallel data output   |
| —               | —          | 12          | N.C.                   | Not connected          |
| —               | —          | 13          | N.C.                   | Not connected          |
| 11              | 12         | 14          | Q7                     | Parallel data output   |
| 12              | 13         | 15          | Q8                     | Parallel data output   |
| 13              | 14         | 16          | Q9                     | Parallel data output   |
| 14              | 15         | 17          | Q10                    | Parallel data output   |
| 15              | 16         | 18          | Q11                    | Parallel data output   |
| —               | 17         | 19          | $\overline{\text{OE}}$ | Output Enable          |
| 16              | 18         | 20          | V <sub>DD</sub>        | Power supply           |

## ●Electrical characteristics (Ta = 25°C)

DC characteristics (unless otherwise noted, Ta = 25°C, V<sub>SS</sub> = 0V)

| Parameter                  | Symbol           | Min. | Typ. | Max.  | Unit | V <sub>DD</sub> | Conditions                                           |
|----------------------------|------------------|------|------|-------|------|-----------------|------------------------------------------------------|
| Input high level voltage   | V <sub>IH</sub>  | 3.5  | —    | —     | V    | 5               | —                                                    |
|                            |                  | 2.5  | —    | —     |      | 3               |                                                      |
| Input low level voltage    | V <sub>IL</sub>  | —    | —    | 1.5   | V    | 5               | —                                                    |
|                            |                  | —    | —    | 0.4   |      | 3               |                                                      |
| Output low level voltage   | V <sub>OL</sub>  | —    | —    | 2.0   | V    | 5               | I <sub>OL</sub> = 20mA                               |
|                            |                  | —    | —    | 1.0   |      | 3               | I <sub>OL</sub> = 5mA                                |
| "H" output disable current | I <sub>OZH</sub> | —    | —    | 10.0  | μA   | 5               | V <sub>O</sub> = 25.0V                               |
| "L" output disable current | I <sub>OZL</sub> | —    | —    | − 5.0 | μA   | 5               | V <sub>O</sub> = 0V                                  |
| Current dissipation        | I <sub>DD</sub>  | —    | —    | 5.0   | μA   | 5               | V <sub>IN</sub> = V <sub>SS</sub> or V <sub>DD</sub> |
|                            |                  | —    | —    | 3.0   |      | 3               | OUTPUT: OPEN                                         |

BU2090 / F / FS switching characteristics (unless otherwise noted, Ta = 25°C, V<sub>SS</sub> = 0V)

| Parameter                 | Symbol            | Min. | Typ. | Max. | Unit | V <sub>DD</sub> | Conditions |
|---------------------------|-------------------|------|------|------|------|-----------------|------------|
| Minimum clock pulse width | t <sub>w</sub>    | 500  | —    | —    | ns   | 5               | —          |
|                           |                   | 1000 | —    | —    |      | 3               |            |
| Data shift setup time     | t <sub>SU</sub>   | 200  | —    | —    | ns   | 5               | —          |
|                           |                   | 300  | —    | —    |      | 3               |            |
| Data shift hold time      | t <sub>H</sub>    | 200  | —    | —    | ns   | 5               | —          |
|                           |                   | 400  | —    | —    |      | 3               |            |
| Data latch setup time     | t <sub>LSUH</sub> | 50   | —    | —    | ns   | 5               | —          |
|                           |                   | 100  | —    | —    |      | 3               |            |
| Data latch hold time      | t <sub>LHH</sub>  | 250  | —    | —    | ns   | 5               | —          |
|                           |                   | 500  | —    | —    |      | 3               |            |
| Data latch "L" setup time | t <sub>LSUL</sub> | 200  | —    | —    | ns   | 5               | —          |
|                           |                   | 400  | —    | —    |      | 3               |            |
| Data latch "L" hold time  | t <sub>LHL</sub>  | 250  | —    | —    | ns   | 5               | —          |
|                           |                   | 500  | —    | —    |      | 3               |            |

○Not designed for radiation resistance.

BU2090 / F / FS switching characteristics measurement conditions

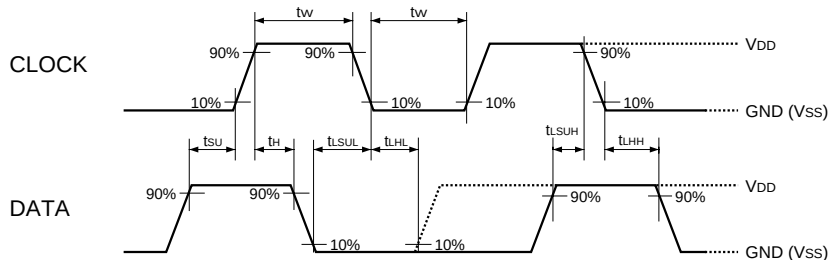


Fig.1

BU2092 / F / FV switching characteristics (unless otherwise noted,  $T_a = 25^\circ\text{C}$ ,  $V_{SS} = 0\text{V}$ )

| Parameter                                     | Symbol                | Min. | Typ. | Max. | Unit | $V_{DD}$ | Conditions                                     |
|-----------------------------------------------|-----------------------|------|------|------|------|----------|------------------------------------------------|
| Transmission delay time<br>(LCK to OUTPUT QX) | $t_{PLZ}(\text{LCK})$ | —    | 55   | —    | ns   | 5        | $R_L = 5\text{k}\Omega$<br>$C_L = 10\text{pF}$ |
|                                               |                       | —    | 90   | —    |      | 3        |                                                |
|                                               | $t_{PZL}(\text{LCK})$ | —    | 50   | —    | ns   | 5        | $R_L = 5\text{k}\Omega$<br>$C_L = 10\text{pF}$ |
|                                               |                       | —    | 115  | —    |      | 3        |                                                |
| Output disable time<br>(OE to OUTPUT QX)      | $t_{PLZ}$             | —    | 45   | —    | ns   | 5        | $R_L = 5\text{k}\Omega$<br>$C_L = 10\text{pF}$ |
|                                               |                       | —    | 70   | —    |      | 3        |                                                |
|                                               | $t_{PZL}$             | —    | 35   | —    | ns   | 5        | $R_L = 5\text{k}\Omega$<br>$C_L = 10\text{pF}$ |
|                                               |                       | —    | 80   | —    |      | 3        |                                                |
| Minimum clock pulse width                     | $t_w$                 | 500  | —    | —    | ns   | 5        | —                                              |
|                                               |                       | 1000 | —    | —    |      | 3        |                                                |
| Minimum latch pulse width                     | $t_w(\text{LCK})$     | 500  | —    | —    | ns   | 5        | —                                              |
|                                               |                       | 1000 | —    | —    |      | 3        |                                                |
| Setup time<br>(LCK to CLOCK)                  | $t_s$                 | 200  | —    | —    | ns   | 5        | —                                              |
|                                               |                       | 400  | —    | —    |      | 3        |                                                |
| Setup time<br>(DATA to CLOCK)                 | $t_{su}$              | 200  | —    | —    | ns   | 5        | —                                              |
|                                               |                       | 400  | —    | —    |      | 3        |                                                |
| Hold time<br>(CLOCK to DATA)                  | $t_h$                 | 200  | —    | —    | ns   | 5        | —                                              |
|                                               |                       | 400  | —    | —    |      | 3        |                                                |

○ Not designed for radiation resistance.

BU2092 / F / FV switching characteristics measurement conditions

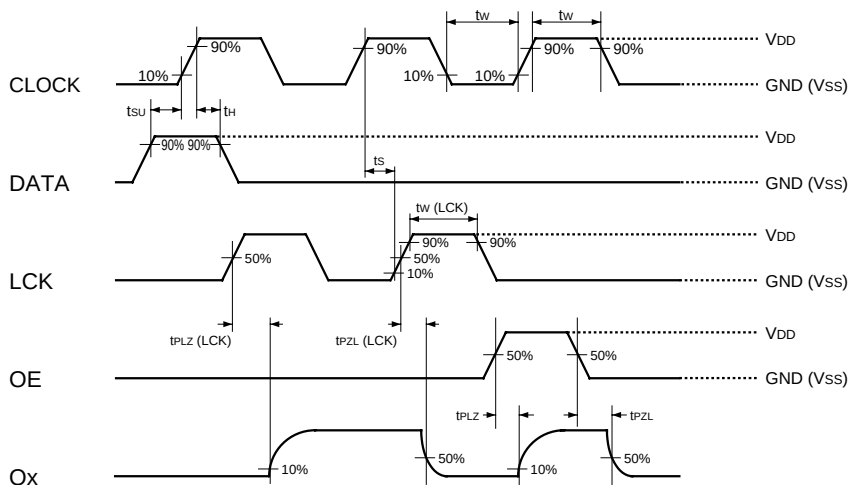


Fig.2

●Truth table  
BU2092 / F / FV

| INPUT                                                                             |      |                                                                                   |    | FUNCTION                                                                                                                                                                         |
|-----------------------------------------------------------------------------------|------|-----------------------------------------------------------------------------------|----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CLOCK                                                                             | DATA | LCK                                                                               | OE |                                                                                                                                                                                  |
| ×                                                                                 | ×    | ×                                                                                 | H  | Output (Q0 to Q11) disabled                                                                                                                                                      |
| ×                                                                                 | ×    | ×                                                                                 | L  | Output (Q0 to Q11) enabled                                                                                                                                                       |
|  | L    | ×                                                                                 | ×  | First cell of the shift register stores the LOW. Other cells, respectively, store data from the preceding cells or other prior data. (Output state is HOLD.)                     |
|  | H    | ×                                                                                 | ×  | First cell of the shift register stores the HIGH. Other cells, respectively, store data from the preceding cells or other prior data. (Storage state and output state are HOLD.) |
|  | ×    | ×                                                                                 | ×  | No change in shift register.                                                                                                                                                     |
| ×                                                                                 | ×    |  | ×  | Contents of shift register are stored in storage register.                                                                                                                       |
| ×                                                                                 | ×    |  | ×  | No change in shift register.                                                                                                                                                     |

Q0 to Q11 output for the BU2090 / F / FS and BU2092 / F / FV is Nch open drain output. When the shift register transfer data is LOW, the corresponding output FET is ON (continuous state). When the transfer data is HIGH, the output FET is OFF (discontinuous).

●Input / output circuit

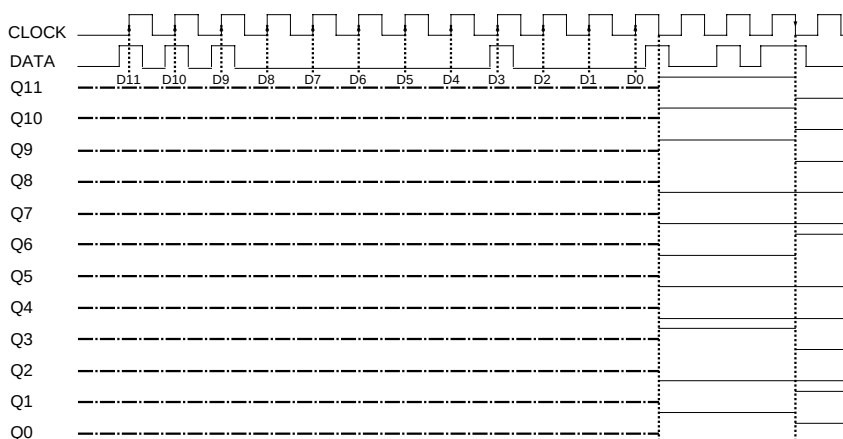
| BU2090 / F / FS |      | BU2092 / F |             | BU2092FV |             | BU2090 / F / FS |                                          | BU2092 / F |                                           | BU2092FV |                                           |
|-----------------|------|------------|-------------|----------|-------------|-----------------|------------------------------------------|------------|-------------------------------------------|----------|-------------------------------------------|
| Pin No.         | 2, 3 | Pin No.    | 2, 3, 4, 17 | Pin No.  | 2, 3, 4, 19 | Pin No.         | 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15 | Pin No.    | 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16 | Pin No.  | 5, 6, 7, 8, 9, 10, 11, 14, 15, 16, 17, 18 |
|                 |      |            |             |          |             |                 |                                          |            |                                           |          |                                           |

### ●Circuit operation

The logic of the DATA pin is sent to the 12-bit shift register on the rising edge of the CLOCK pulse. Subsequently, it is shifted from Q0 to Q11 for every clock rising edge.

For the BU2090 / F / FS

When the DATA pin is LOW on the CLOCK falling edge, the data does not change its output state. It is only shifted in the internal shift register. However, when the DATA pin is HIGH, the content of the 12-bit shift register is latched and is output to the corresponding Q0 to Q11.



Note 1) — indicates unstable output.

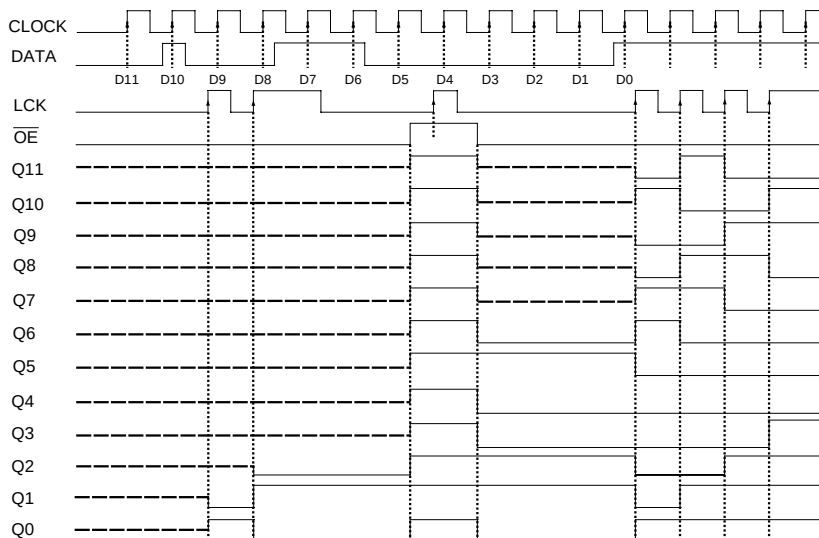
Note 2) Pull-up resistance is connected to the output pin.

Fig.3 Operation timing chart



For the BU2092 / F / FV

The content of the 12-bit shift register is stored in the 12-bit storage register at the rising edge of LCK, and is output to the corresponding Q0 to Q11. When OE is HIGH, regardless of the content of the storage register, the output FET turns OFF and enters a HIGH (discontinuous) state.



Note 1) — indicates unstable output.

Note 2) Pull-up resistance is connected to the output pin.

Fig.4 Operation timing chart

## ●Application example

BU2090 / F / FS

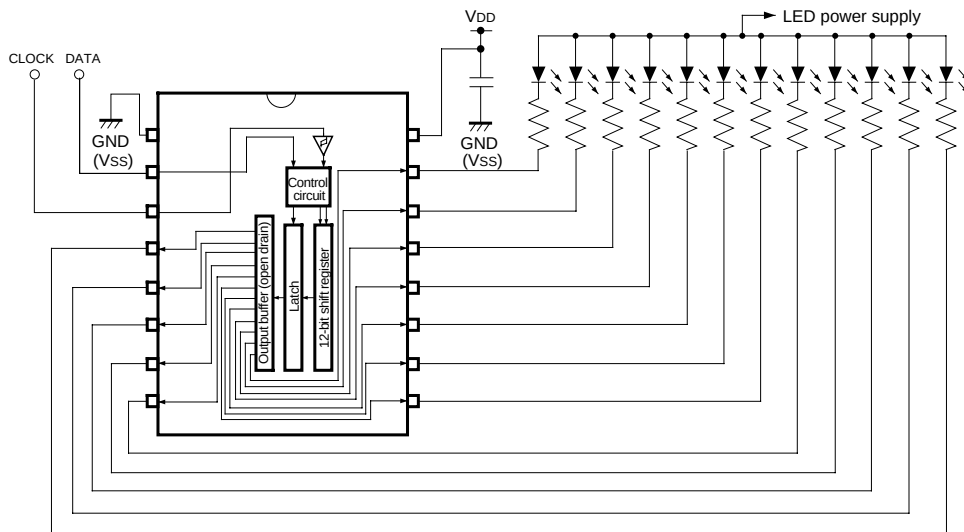


Fig.5

BU2092 / F / (FV)

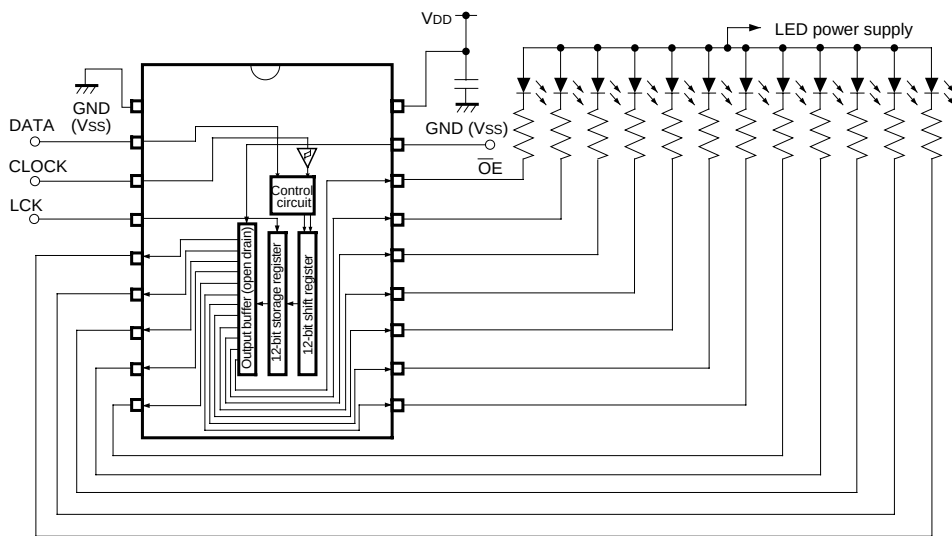


Fig.6

●Electrical characteristic curves

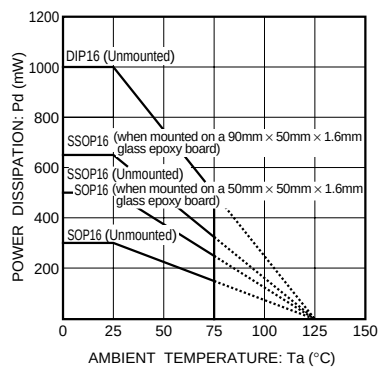


Fig.7 BU2090 / F / FS thermal derating characteristics

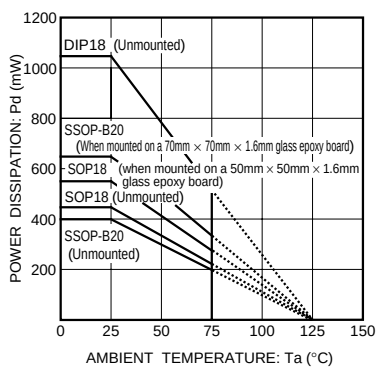


Fig.8 BU2092 / F / FV thermal derating characteristics

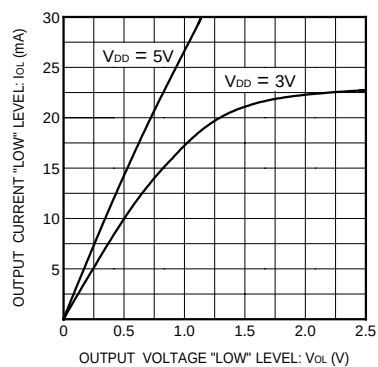
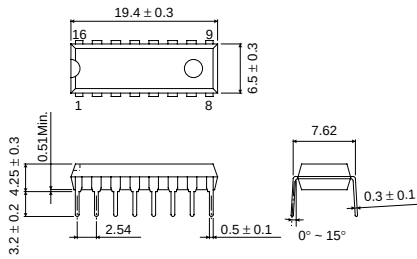


Fig.9 Output current vs.output low level voltage

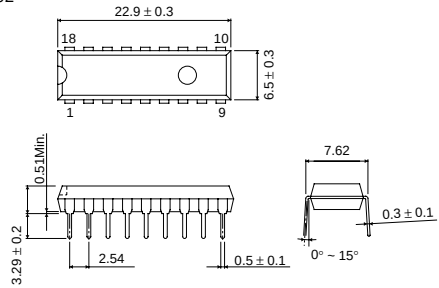
## ●External dimensions (Units: mm)

BU2090



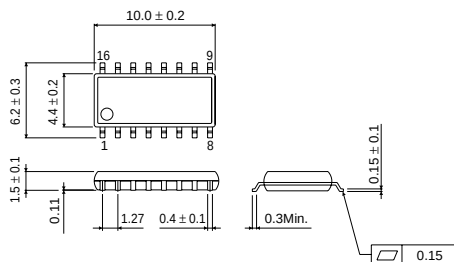
DIP16

BU2092



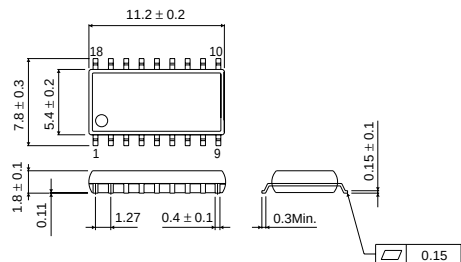
DIP18

BU2090F



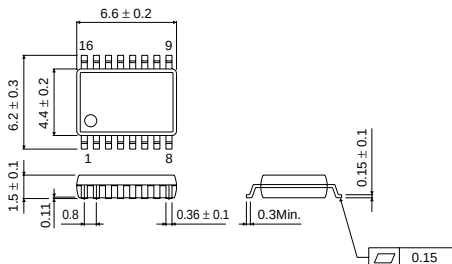
SOP16

BU2092F



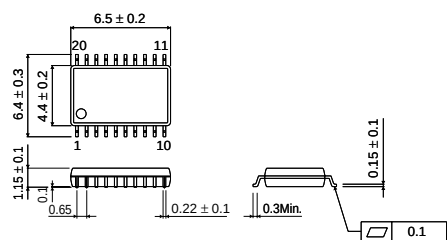
SOP18

BU2090FS



SSOP-A16

BU2092FV



SSOP-B20