DC Characteristics (Cont.)

Program, Program Verify, and Program Inhibit Modes
T_a = 25°C ± 5°C; V_{CC} = +5V ± 5%; V_{PP} = +21V ± 0.5V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input High Voltage	V_{IH}	2.0		V_{CC} + 1	V	
Input Low Voltage	V_{IL}	−0.1		0.8	V	
Input Leakage Current	I_{LI}			10	µA	$V_{IN} = V_{IL}$ or V_{IH}
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −400µA
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.1mA
V_{CC} Current	I_{CC}		85	125	mA	
V_{PP} Current	I_{PP}			30	mA	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{PP}$

AC Characteristics

Read Mode and Standby Mode
T_a = 0°C to +70°C; V_{CC} = +5V ± 5%

Parameter	Symbol	Limits 2732A-2 Min	Typ	Max	2732A Min	Typ	Max	2732A-3 Min	Typ	Max	Unit	Test Conditions
Address to Output Delay	t_{ACC}			200			250			300	ns	$\overline{CE}$ = $\overline{OE}/V_{PP} = V_{IL}$
CE to Output Delay	t_{CE}		200			250			300		ns	$\overline{OE} = V_{IL}$
Output Enable to Output Delay	t_{OE}		70			100			150		ns	$\overline{CE} = V_{IL}$
Output Enable High to Output Float	t_{DF}		60			90			130		ns	$\overline{CE} = V_{IH}$
Address to Output Hold	t_{OH}	0			0			0			ns	$\overline{CE}$ = $\overline{OE} = V_{IL}$

Test Conditions —
Output Load: 1 TTL gate and C_L = 100pF
Input Rise and Fall Times: 20ns
Input Pulse Levels: 0.8V to 2.2V
Timing Measurement Reference Levels:
Inputs: 1.0V and 2.0V
Outputs: 0.8V and 2.0V

Program, Program Verify, and Program Inhibit Modes
T_a = 25°C ± 5°C; V_{CC} = +5V ± 5%; V_{PP} = +21V ± 0.5V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Address Setup Time	t_{AS}	2			µs	
OE Setup Time	t_{OES}	2			µs	
Data Setup Time	t_{DS}	2			µs	
Address Hold Time	t_{AH}	0			µs	
OE Hold Time	t_{OEH}	2			µs	
Data Hold Time	t_{DH}	2			µs	
Output Enable to Output Float Delay	t_{DF}	0		130	ns	
Data Valid from CE	t_{DV}			1	µs	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IL}$
Program Pulse Width	t_{PW}	45	50	55	ms	
Program Pulse Rise Time	t_{PRT}	50			ns	
V_{PP} Recovery Time	t_{VR}	2			µs	

Test Conditions —
Input Pulse Levels: 0.8V to 2.2V
Input Timing Reference Levels: 1.0V and 2.0V
Output Timing Reference Levels: 0.8V and 2V
Input Rise and Fall Times: 20ns

Function

The µPD2732A operates from a single +5V power supply, making it ideal for microprocessor applications.

Programming of the µPD2732A is achieved with a single 50ms TTL pulse. Total programming time for all 32,768 bits is only 210 seconds. Due to the simplicity of the programming requirements, devices on boards and in systems may be easily programmed without any special programmer.

The µPD2732A features a Standby mode which reduces the power dissipation from a maximum active power dissipation of 656mW to a maximum standby power dissipation of 158mW. This results in a 75% savings with no increase in access time.

Erasure of the µPD2732A programmed data can be attained when exposed to light with wavelengths shorter than approximately 4,000 Angstroms (Å). It should be noted that constant exposure to direct sunlight or room level fluorescent lighting could erase the µPD2732A. Consequently, if the µPD2732A is to be exposed to these types of lighting conditions for long periods of time, its window should be masked to prevent unintentional erasure.

The recommended erasure procedure for the µPD2732A is exposure to ultraviolet light with wavelengths of 2,537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be not less than 15W-sec/cm^2. The erasure time is approximately 15 to 20 minutes using an ultraviolet lamp of 12,000µW/cm^2 power rating.

During erasure, the µPD2732A should be placed within 1 inch of the lamp tubes. If the lamps have filters on the tubes, the filters should be removed before erasure.

Operation

The five operation modes of the µPD2732A are listed in Table 1. In the Read mode the only power supply required is a +5V supply. During programming, all inputs are TTL levels except for $\overline{OE}/V_{PP}$ which is pulsed from TTL level to 21V.

Read Mode

When $\overline{CE}$ and $\overline{OE}/V_{PP}$ are at a low (0) level, read is set and data is available at the outputs after t_{OE} from the falling edge of $\overline{OE}$ and t_{ACC} after setting the address.

Standby Mode

The µPD2732A is placed in a Standby mode with the application of a high (1) level TTL signal to the $\overline{CE}$ input. In this mode, the outputs are in a high impedance state, independent of the $\overline{OE}/V_{PP}$ input. The active power dissipation is reduced by 75% from 656mW to 158mW.

Program Mode

Programming begins by erasing all data and consequently having all bits in the high (1) level state. Data is then entered by programming a low (0) level TTL signal into the chosen bit location.

The µPD2732A is placed in the Program mode by applying a high (1) level TTL signal to the $\overline{CE}$ and with $\overline{OE}/V_{PP}$ at +21V. The data to be programmed is applied to the output pins in 8-bit parallel form at TTL levels.

Any location can be programmed at any time, either individually, sequentially, or at random.

When multiple µPD2732As are connected in parallel, except for $\overline{CE}$, individual µPD2732As can be programmed by applying a low (0) level TTL pulse to the $\overline{CE}$ input of the desired µPD2732A to be programmed.

Programming of multiple µPD2732As in parallel with the same data is easily accomplished. All the like inputs are tied together and programmed by applying a low (0) level TTL pulse to the $\overline{CE}$ inputs.

Program Inhibit Mode

Programming multiple µPD2732As in parallel with different data is easier with the Program Inhibit mode. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel µPD2732As may be common. Programming is accomplished by applying the TTL-level program pulse to the $\overline{CE}$ input with $\overline{OE}/V_{PP}$ at +21V. A high (1) level applied to the $\overline{CE}$ of the other µPD2732A will inhibit it from being programmed.