

HD74LS374

Octal D-type Edge-triggered Flip-Flops (with three-state outputs)

REJ03D0483-0200

Rev.2.00

Feb.18.2005

The HD74LS374, 8-bit register features totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide this register with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. The eight flip-flops are edge-triggered D-type flip-flops. On the positive transition the clock, the Q outputs will be set to the logic states that were setup at the D inputs.

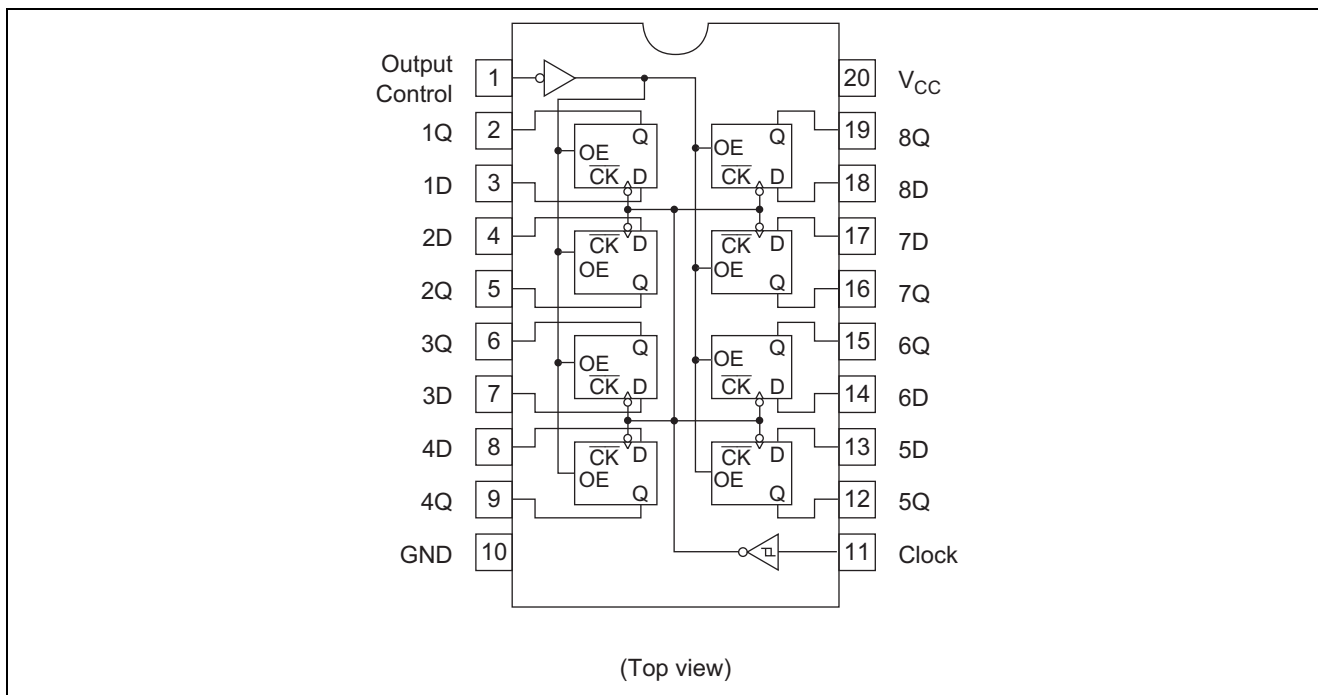
Features

- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS374P	DILP-20 pin	PRDP0020AC-B (DP-20NEV)	P	—
HD74LS374FPEL	SOP-20 pin (JEITA)	PRSP0020DD-B (FP-20DAV)	FP	EL (2,000 pcs/reel)
HD74LS374RPEL	SOP-20 pin (JEDEC)	PRSP0020DC-A (FP-20DBV)	RP	EL (1,000 pcs/reel)

Note: Please consult the sales office for the above package availability.

Pin Arrangement



Function Table

Inputs			Outputs
Output control	Clock	D	Q
L	$\uparrow$	H	H
L	$\uparrow$	L	L
L	L	X	Q_0
H	X	X	Z

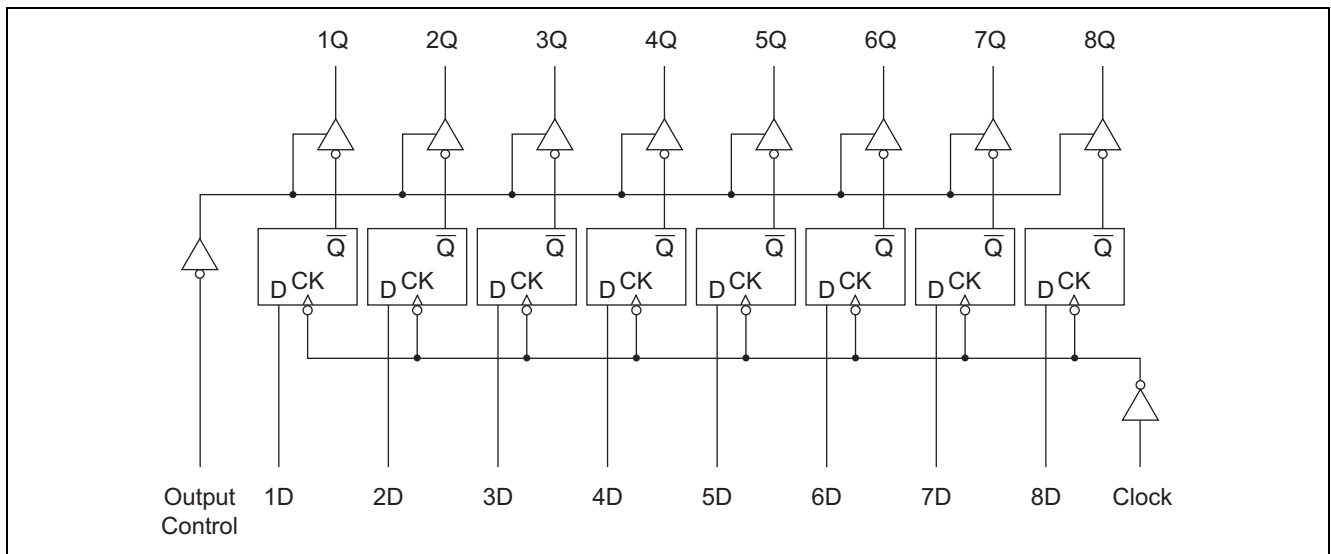
Notes: H; high level, L; low level, X; irrelevant

$\uparrow$; transition from low to high level

Q_0 ; level of Q before the indicated steady state input conditions were established

Z; off (high-impedance) state of a three state output

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	7	V
Input voltage	V_{IN}	7	V
Power dissipation	P_T	400	mW
Storage temperature	T_{stg}	-65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output voltage	V_{OH}	—	—	5.5	V
Output current	I_{OH}	—	—	-2.6	mA
	I_{OL}	—	—	24	mA
Operating temperature	T_{opr}	-20	25	75	°C
Clock pulse width	"H" Level	15	—	—	ns
	"L" Level	15	—	—	ns
Data setup time	t_{su}	20 $\uparrow$	—	—	ns
Data hold time	t_h	0 $\uparrow$	—	—	ns

Electrical Characteristics

(Ta = -20 to +75 °C)

Item	Symbol	min.	typ.*	max.	Unit	Condition
Input voltage	V _{IH}	2.0	—	—	V	
	V _{IL}	—	—	0.8	V	
Output voltage	V _{OH}	2.4	—	—	V	V _{CC} = 4.75 V, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -2.6 mA
	V _{OL}	—	—	0.4	V	V _{CC} = 4.75 V, I _{OL} = 12 mA
		—	—	0.5		
Output current	I _{OZH}	—	—	20	μA	V _O = 2.7 V
	I _{OZL}	—	—	-20		V _O = 0.4 V
						V _{CC} = 5.25 V, V _{IH} = 2 V, V _{IL} = 0.8 V
Input current	I _{IH}	—	—	20	μA	V _{CC} = 5.25 V, V _I = 2.7 V
	I _{IL}	—	—	-0.4	mA	V _{CC} = 5.25 V, V _I = 0.4 V
	I _I	—	—	0.1	mA	V _{CC} = 5.25 V, V _I = 7 V
Short-circuit output current	I _{OS}	-30	—	-130	mA	V _{CC} = 5.25 V
Supply current	I _{CC}	—	27	40	mA	V _{CC} = 5.25 V, V _I = 4.5 V (Output control)
Input clamp voltage	V _{IK}	—	—	-1.5	V	V _{CC} = 4.75 V, I _{IN} = -18 mA

Note: * V_{CC} = 5 V, Ta = 25°C

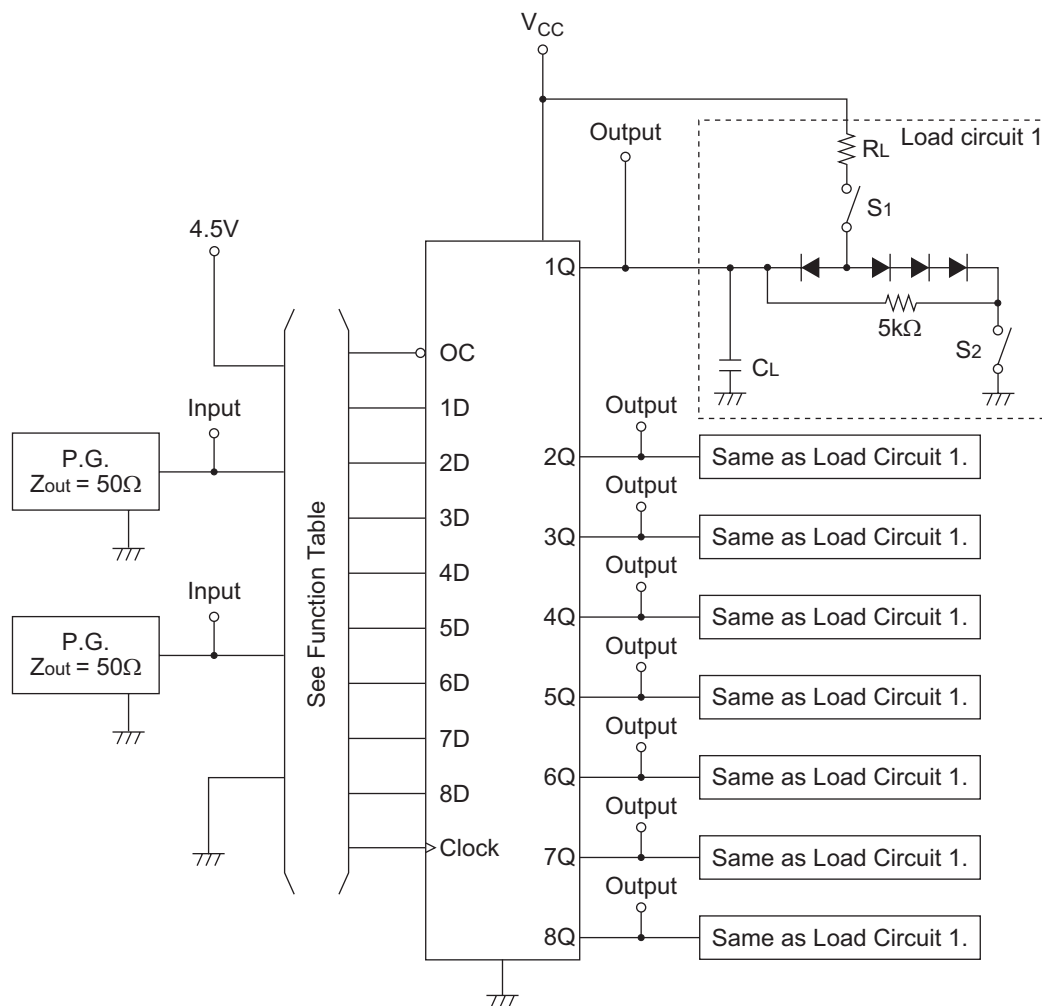
Switching Characteristics

(V_{CC} = 5 V, Ta = 25°C)

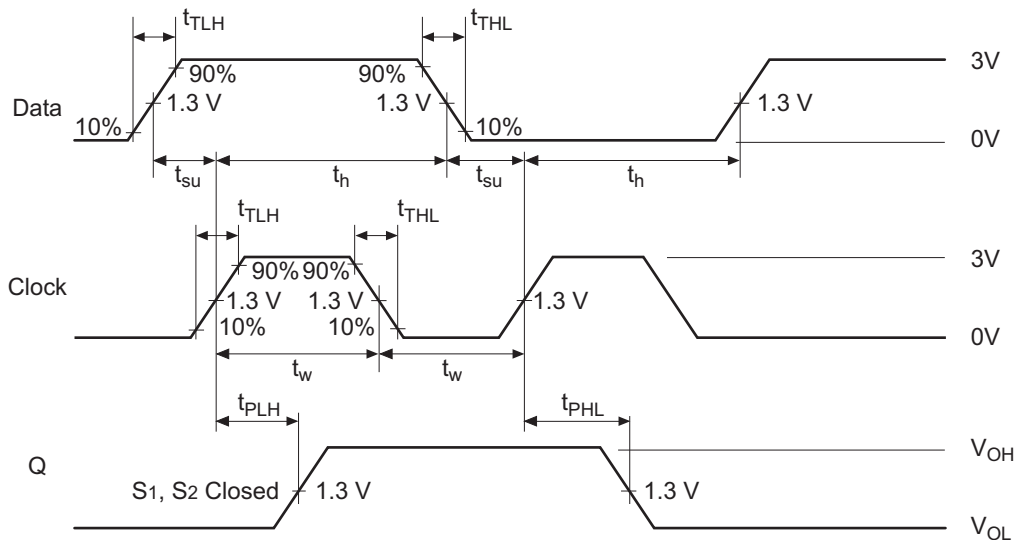
Item	Symbol	Inputs	Output	min.	typ.	max.	Unit	Condition
Maximum clock frequency	f _{max}	Clock	Q	35	50	—	MHz	
Propagation delay time	t _{PLH}	Clock	Q	—	15	28	ns	C _L = 45 pF, R _L = 667 Ω
	t _{PHL}			—	19	28		
Output enable time	t _{ZH}	OC	Q	—	20	28		
	t _{ZL}			—	21	28		
Output disable time	t _{HZ}	OC	Q	—	12	20		C _L = 5 pF, R _L = 667 Ω
	t _{LZ}			—	14	25		

Testing Method

Test Circuit

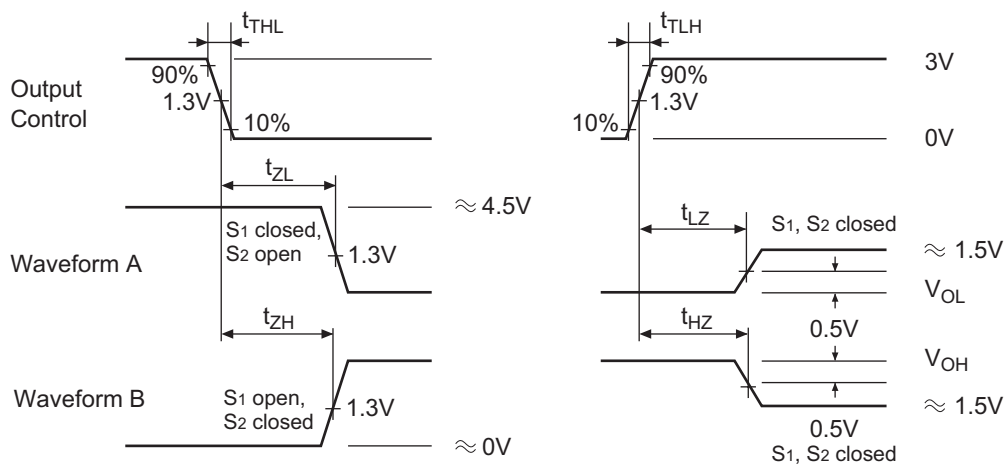


Waveforms 1



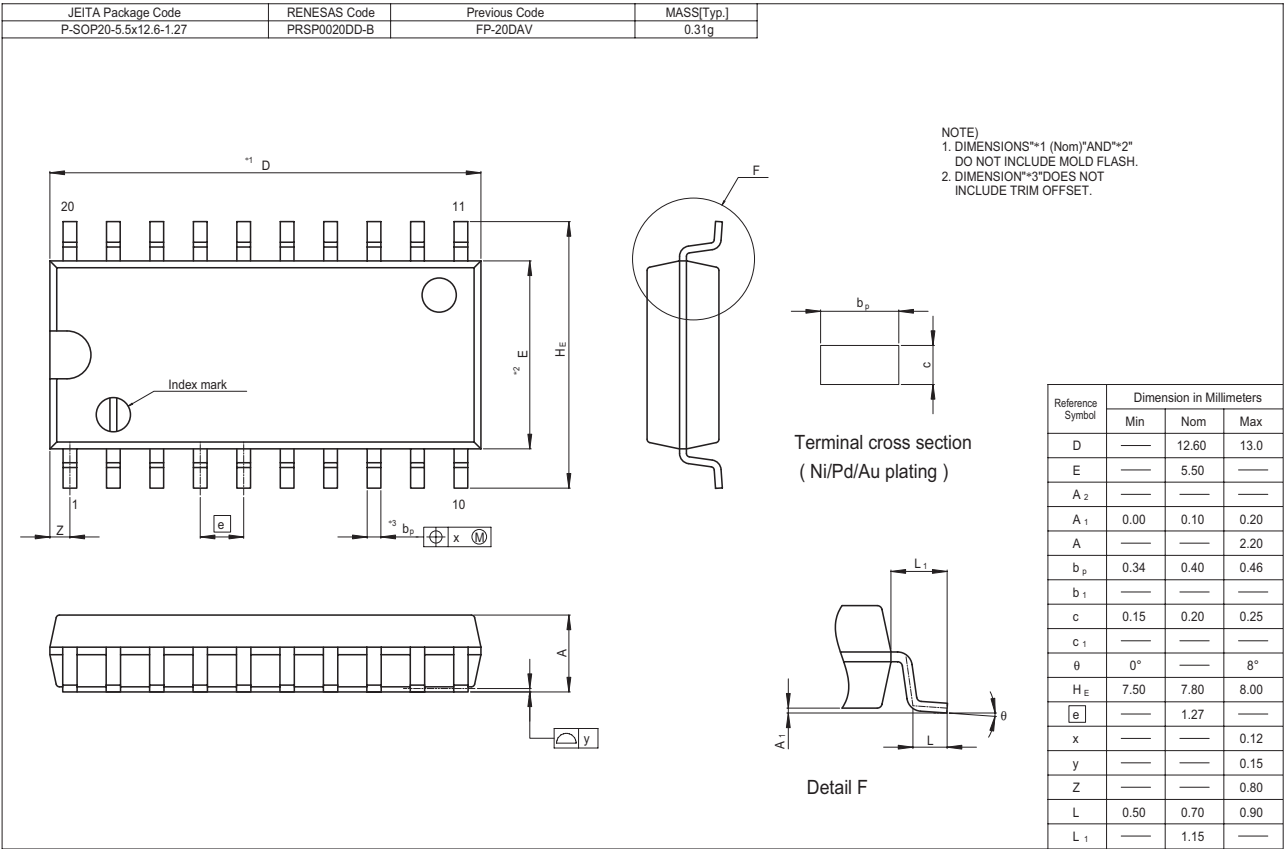
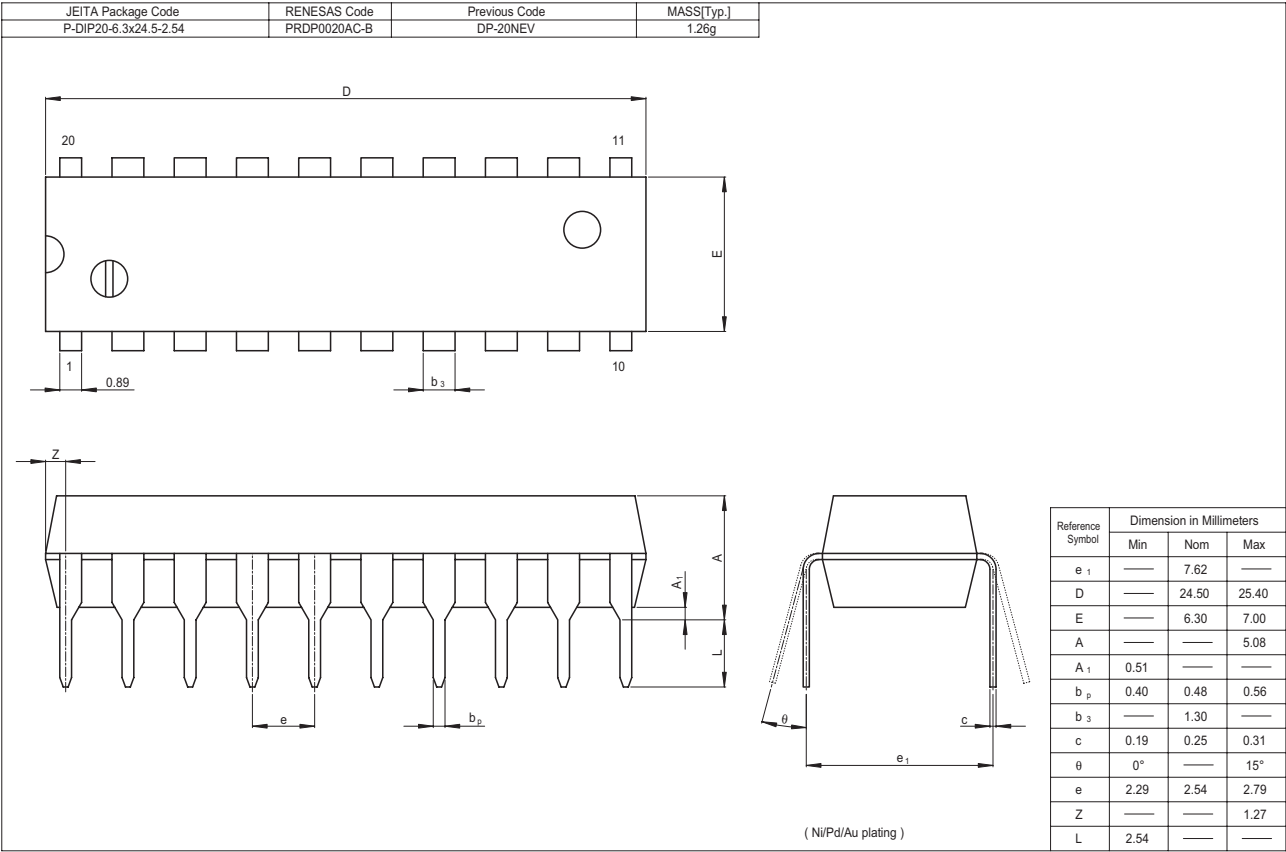
- Notes:
1. Input pulse; $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns
Clock input; PRR = 1 MHz, duty cycle 50%
Data input pulse; PRR = 500 kHz, duty cycle 50%
 2. f_{max} : $t_{TLH} \leq 2.5$ ns, $t_{THL} \leq 2.5$ ns

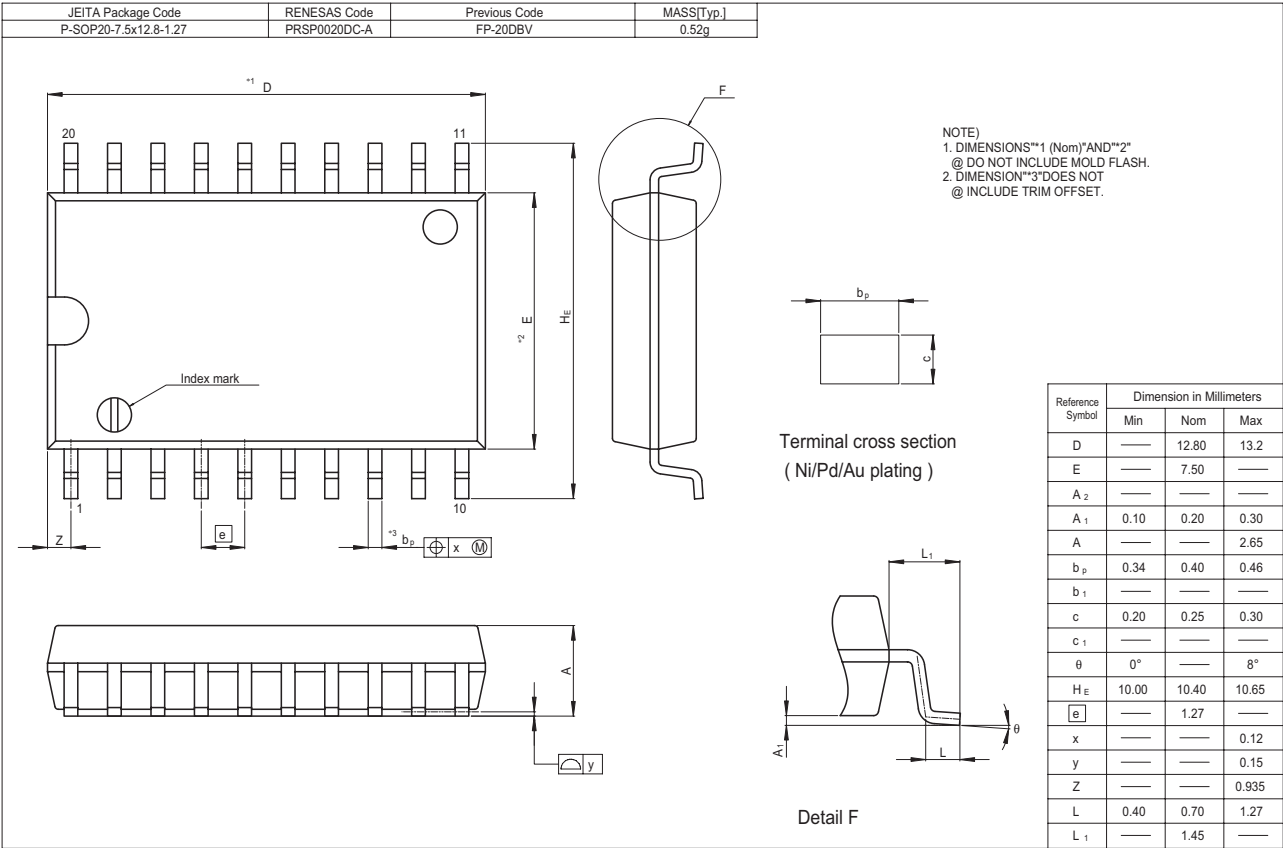
Waveforms 2



- Notes:
1. Input pulse; $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns, PRR = 1 MHz, duty cycle 50%
 2. Waveform A is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform B is for an output with internal conditions such that the output is high except when disabled by the output control.

Package Dimensions





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